AN10958

Fluorescent lamp driver with PFC using the UBA2015/16 family

Rev. 1 — 20 June 2011 **Application note**

Document information

Info	Content
Keywords	UBA2015, UBA2015A, UBA2016A fluorescent lamp driver, PFC
Abstract	This Application note describes designs using IC family UBA2015, UBA2015A and UBA2016A for common ballast topologies. The IC is a controller used in electronic ballast for fluorescent lamps incorporating controllers and NMOST drivers for Power Factor Correction (PFC) and the half-bridge circuit. The fluorescent lamp ballast controller is a high-voltage controller which is capable of driving a zero-voltage switching resonant topology. The lamp controller module includes a high-voltage level shift circuit and several protection features, such as hard switching/capacitive mode protection, half-bridge overcurrent (coil saturation) protection, lamp overvoltage (lamp removal) protection and temperature protection. In addition to the lamp controller, the IC also contains a PFC controller. Efficient operation of the PFC is obtained by the quasi-resonant operation with valley skipping. Overcurrent protection, overvoltage protection and demagnetization sensing ensures safe operation in all conditions. The brownout protection of the PFC controller reduces the half-bridge frequency to prevent excessive currents. The proprietary high-voltage BCD-Powerlogic process enables efficient, direct start-up from the rectified universal mains voltage. The IC can drive half-bridge circuits with a supply voltage up to 600 V (AC). The combination of PFC and lamp controller makes the IC very suitable for fluorescent ballasts with either a dimmable or fixed lamp current output, with a PFC for AC mains voltages up to 390 V.

Revision history

Rev	Date	Description
v.1	20110620	initial version

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1. Introduction

1.1 General IC description

Today's market demands high-quality, reliable, lightweight, small and efficient electronic High Frequency (HF) ballast with lamp end-of-life detection. The high-end market segment also requires dimming functionality.

Electronic ballasts provide high efficiency performance because the lamp is operated at high frequencies between 10 kHz and 100 kHz and the lamp is more efficient when compared to operation at 50/60 Hz with a magnetic ballast. High frequency operation enables the magnetic components in the electronic ballast to be smaller and therefore electronic ballasts are about one fifth of the weight of magnetic ballasts.

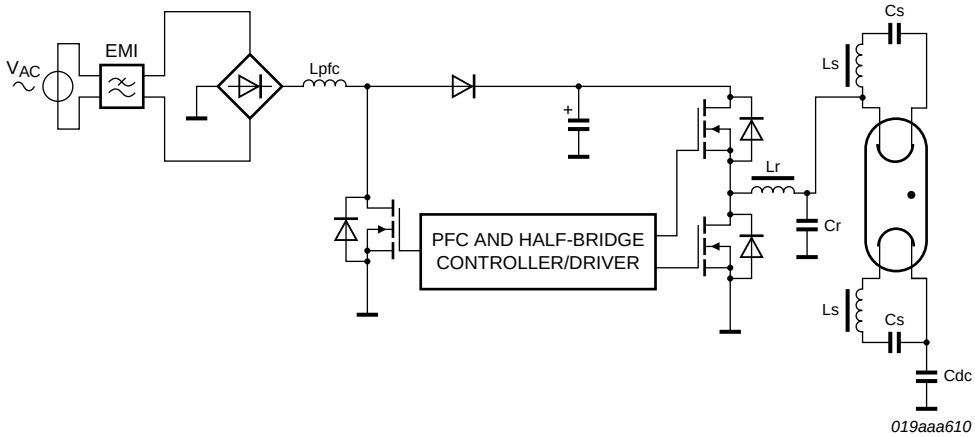
The UBA2015, UBA2015A and UBA2016A combines Power Factor Correction (PFC) and half-bridge controller in one IC which reduces the component cost significantly and increases reliability. It has several protection mechanisms such as overvoltage/no ignition, coil saturation, overtemperature and, on some pins, open/short protection to guarantee reliable and safe operation.

The integrated dimming option allows control of the lamp current down to 1 % of the nominal lamp current. The integrated double-sided rectification of the lamp current feedback signal and a control loop compensation network pin allows stable lamp operation and achieves good dimming performance.

The IC is intended for fluorescent lamp ballast with fixed or dimmable light output, with PFC for AC mains voltages up to 390 V.

A feature list, block diagram and flow chart for the IC are provided in the IC data sheet.

1.2 Basic electronic ballast circuit



The feedback signals are not shown.

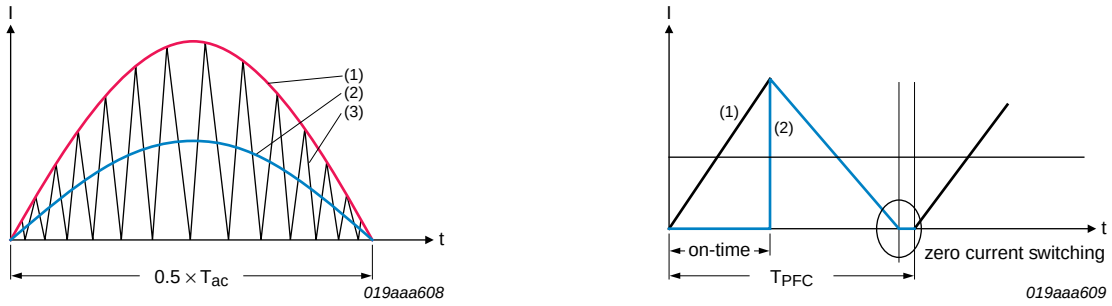
Fig 1. Basic electronic ballast circuit for inductive heating topology

1.2.1 Power factor correction

Lighting applications above 25 W need a PFC circuit to fulfill the Total Harmonic Distortion (THD) and Power Factor (PF) requirements. The PFC circuit is actually a boost or step-up converter, therefore the output voltage must be higher than the peak AC mains voltage. The PFC provides a fixed DC output voltage which helps to create a better defined half-bridge circuit and therefore longer lamp life. A high DC voltage also results in more efficient ballasts for lamps operating at higher voltages.

The PFC operates at a fixed on-time over one mains cycle which forces the peak current of the PFC circuit inductor to follow the sinusoidal mains waveform. The EMI filtering averages the PFC switching current and blocks common mode currents; see Figure 2.

The maximum switching frequency of the PFC circuit is limited by the IC to 133 kHz for easy EMI design but also to reduce switching losses using valley skipping which is very effective at low AC mains input voltage and medium to low output load conditions.



a. Half AC mains cycle

(1) $I_{LPFC(peak)}$.

(2) I_{LPFC}.

(3) $I_{ac(avg)}$.

b. PFC switching cycle

(1) I_{QPFC}.

(2) I_{DPFC}.

Fig 2. PFC circuit currents

A fixed output voltage has the advantage that the half-bridge circuit can be designed for a high input voltage. This makes the half-bridge design more efficient for lamps with a high operating voltage such as T5 lamps.

1.2.2 Inductive heating half-bridge and ballast

Refer to Figure 1. The capacitor (Cr) across the lamp is the resonant capacitor and inductor (Lr) is the resonant inductor. The capacitor in series with the lamp is the DC blocking capacitor (Cdc). Before ignition, the lamp's electrodes are preheated at a predefined half-bridge current (UBA2016A) or frequency (UBA2015).

After preheat, the lamp voltage increases while sweeping the half-bridge operating frequency down to the resonant frequency. Finally, the lamp ignites when the lamp ignition voltage is reached. In case the lamp does not ignite the switching frequency ramp down is stopped to avoid damage to components and a new ignition attempt is started. After a maximum of two ignition attempts the IC enters a standby mode.

Once the lamp is ignited, the resonant tank and switching frequency limit the amount of current through the lamp. The lamp current is controlled by the operating frequency of the half-bridge.

1.2.3 IC family overview

The IC family of half-bridge controller ICs comprise three functionally different versions. All three versions are available in SO20 and DIP20 packages. The functional differences are explained in Table 1.

Table 1. IC family overview

Function	UBA2015	UBA2015A	UBA2016A
PFC controller	yes	yes	yes
Preheat operation	current controlled and fixed frequency	current controlled and fixed frequency	current controlled
Boost function	no	no	yes
Dim function	no	yes	yes

1.2.3.1 Preheat operation

The current controlled preheat operation is intended for conventional series -resonant topology where the half-bridge current is equal to the filament currents. The accuracy of the preheat current is independent of the tolerances of the LC tank and therefore the preheat frequency can be closer to the maximum allowed voltage during preheat. As a result the preheat current can be higher than with fixed frequency preheat.

The fixed frequency preheat operation is intended for multi-lamp ballasts where the total half-bridge current is not equal to the filament current. For example: when a lamp is removed in a two-lamp ballast with conventional series-resonant topology the half-bridge current is reduced by a factor of two.

1.2.3.2 Boost function

The boost function, intended to provide rapid run-up time of light output, is mainly used for amalgam lamps or outdoor applications. The “run-up time” is defined as the time needed by the discharge lamp to reach an output of 80 % of the nominal light output. The boost function allows the lamp to be operated at 1.5 to 2.0 times the lamp’s nominal current. As a result the lamp reaches the optimum operating temperature sooner. The boost is applied at ballast power-on; the boost time is determined by a capacitor in the application.

1.2.3.3 Dim function

The dim function is intended for energy harvesting or light reduction.

2. Basic circuit description

This section describes the deep dimming ballast in the inductive series-resonant topology shown in Figure 1. The inductors Ls and Lr are coupled, therefore the current through the filaments is inductively coupled to the current through Lr in the LC tank.

A complete electronic schematic of a ballast with dimming and boosting using the UBA2016A is shown in Figure 3. This application note uses this schematic as a guide.

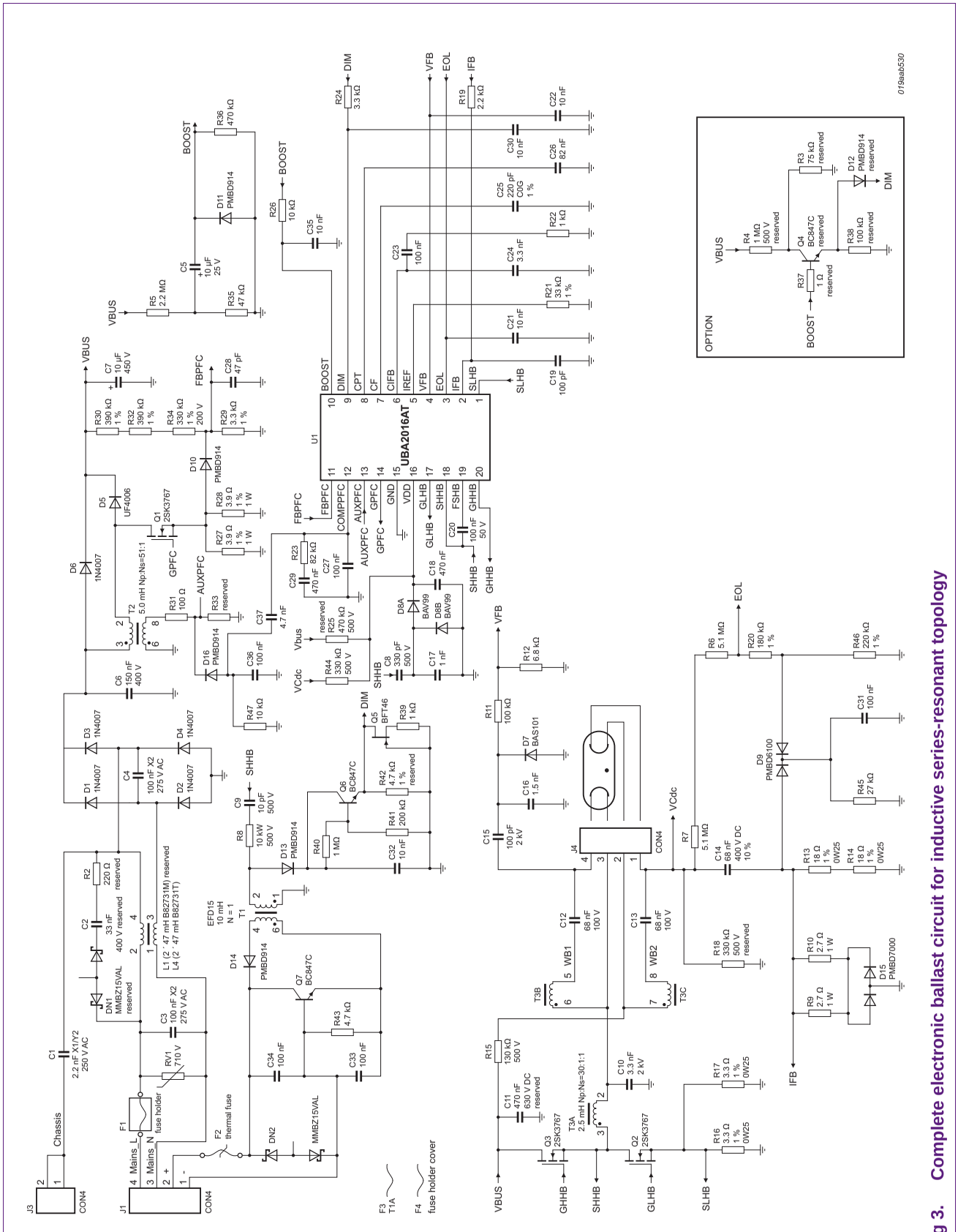


Fig 3. Complete electronic ballast circuit for inductive series-resonant topology

The circuit diagram of the PFC section is shown in Figure 4. Signal FBPFC is the feedback to the controller. The bus voltage VBUS connects to the half-bridge circuit. The AUXPFC signal is fed to the controller. The GPFC is the gate drive signal from the controller.

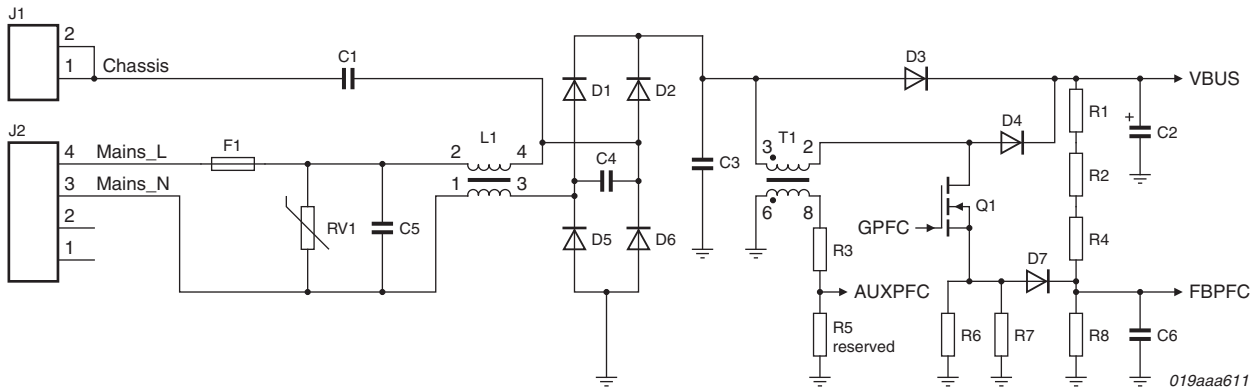


Fig 4. PFC section

The inductive mode series-resonant topology is shown in Figure 5. The electrodes are heated by an inductor coupled to the resonant inductor. The bus voltage is from the PFC circuit output. GHHB and GLHB are the gate drive signals from the controller. SHHB is connected to the input of the controller and provides a supply for the controller during oscillation states. SLHB is connected to the input of the controller. The VFB signal is the lamp voltage feedback. IFB is the lamp current feedback. EOL is the feedback of the DC blocking capacitor C12. The VCdc signal provides the startup current to pin VDD.

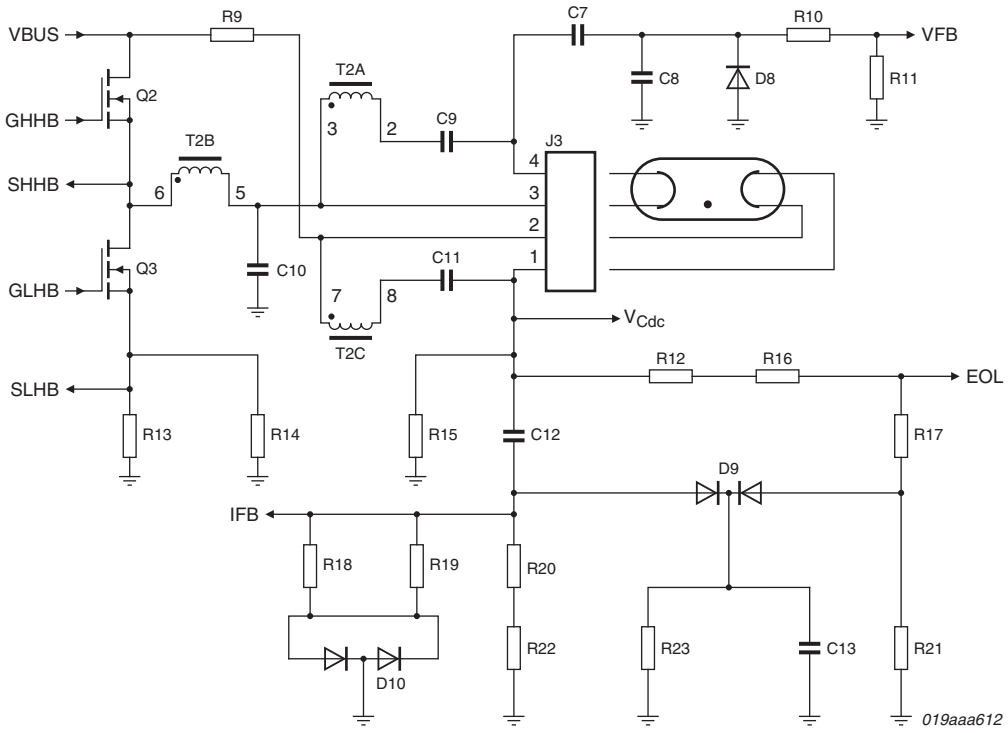


Fig 5. Half-bridge section inductive mode series-resonant topology

The circuit diagram of the PFC and half-bridge controller is shown in Figure 6. AUXPFC, FBPFC and GPFC connect to the PFC circuit. Pin VDD receives the startup current from V_{Cdc} (support re-lamp) or VBUS (no support for re-lamp). During oscillation states, pin VDD is supplied by the dVdt supply generated by signal SHHB. The signals SHHB, GHHB, GLHB, and SLHB connect to the half-bridge NMOSTs. The boost signal is generated from the VBUS voltage. The DIM signal is generated by the dimming input circuit. The VFB signal is the lamp voltage feedback signal. IFB is the lamp current feedback signal. EOL is the voltage of the DC blocking capacitor used for lamp end-of-life detection. The startup resistor R31 can also be connected to the output of the mains bridge rectifier to reduce the power cycle time in case a large value bus capacitor C2 in Figure 4 is required.

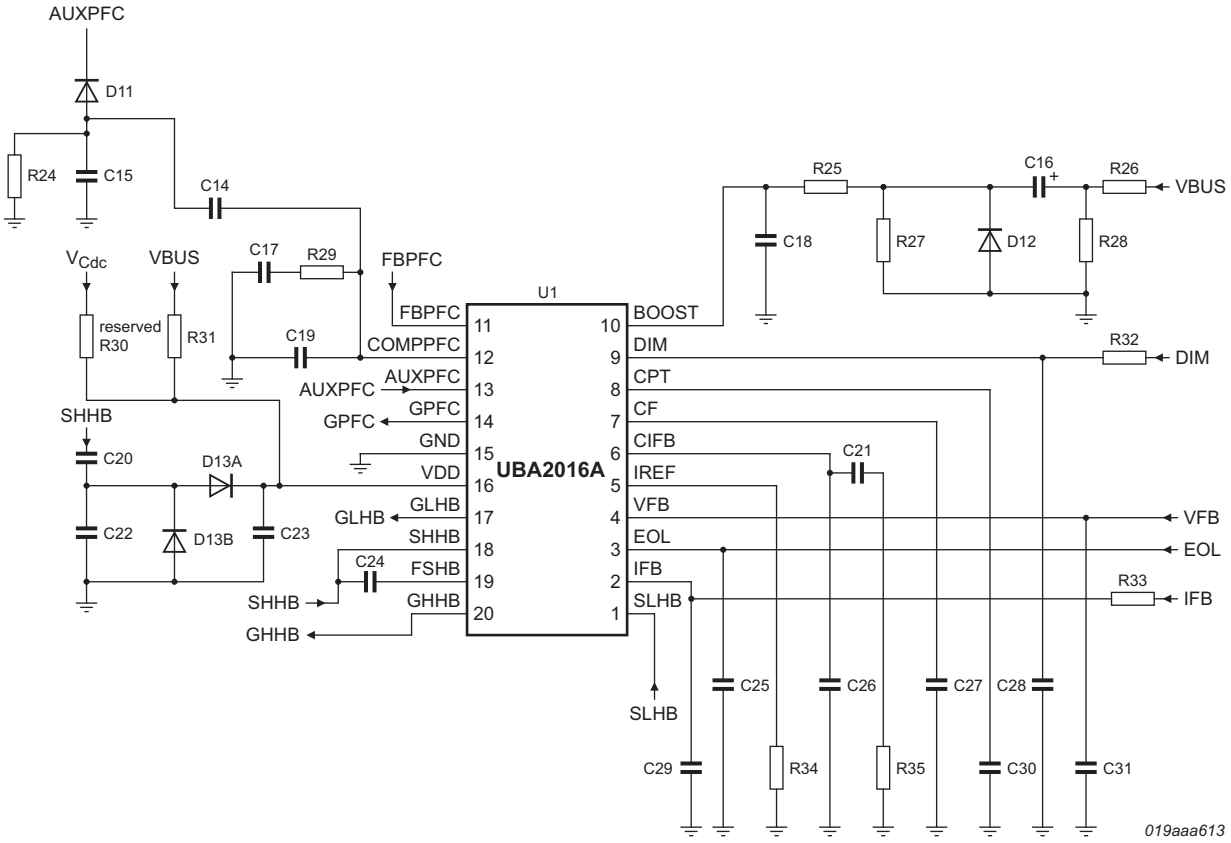


Fig 6. Controller section

The dim control input circuit is described in Figure 7. An AC current from node SHHB of the half-bridge circuit is fed through the galvanic isolation transformer T3. The voltage from an external DC voltage source of 0 V to 10 V can be connected to the user side of T3. Due to the current through T3, the transformer voltage is clamped to the input voltage. The clamped voltage is sensed on the ballast side of T3 and filtered. The DIM signal is fed to the controller.

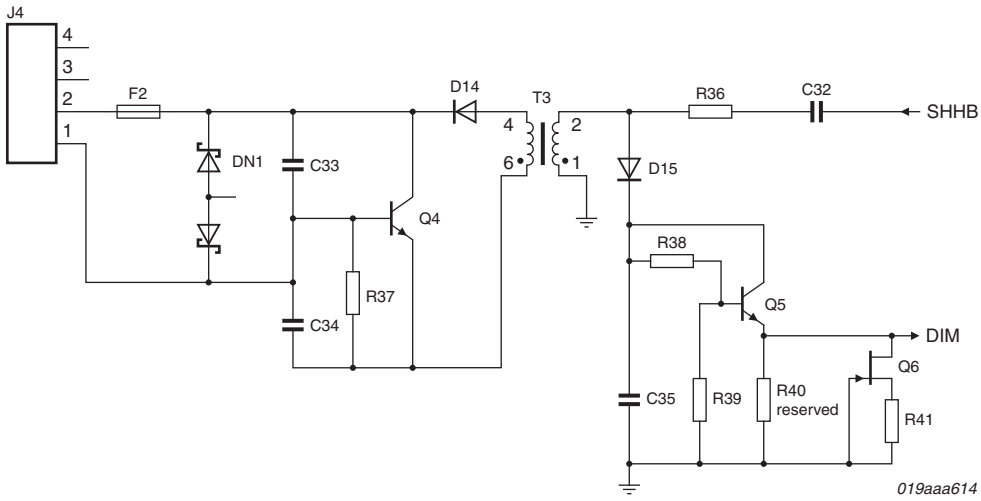


Fig 7. Dim control input section

3. Pin-to-pin component selection

The functionality of the ballast circuit sub-blocks is described in Table 2 to Table 4 based on the functions assigned to each pin.

Table 2. PFC function pins

Symbol	Pin	Description
FBPFC	11	PFC voltage feedback, overvoltage protection, overcurrent protection, open/short protection; see Section 3.12 on page 32
COMPPFC	12	PFC voltage control loop compensation network, input of on-time modulator; see Section 3.13 on page 34
AUXPFC	13	demagnetization detection, THD wave shaping, open pin protection; see Section 3.14 on page 34.
GPFC	14	PFC gate drive; see Section 3.15 on page 35

Table 3. Half-bridge function pins

Symbol	Pin	Description
SLHB	1	preheat current regulation, coil saturation protection; see Section 3.1 on page 12
IFB	2	lamp current feedback input, lamp-on detection, internal lamp current rectifier, lamp overcurrent detection; see Section 3.2 on page 14
EOL	3	lamp end-of-life detection; see Section 3.3 on page 19
VFB	4	lamp voltage feedback, lamp overvoltage detection, open/short protection; see Section 3.4 on page 22
CIFB	6	input of the internal VCO, time constant of the lamp current control loop, ignition frequency ramp down speed after preheat; Section 3.6 on page 24
CF	7	timing capacitor of oscillator; Section 3.7 on page 25

Table 3. Half-bridge function pins

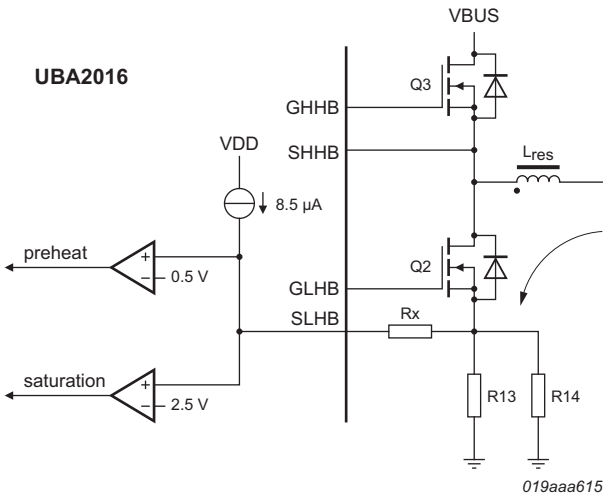
Symbol	Pin	Description
CPT	8	preheat timer, fault timer, open/short protection; see Section 3.8 on page 26
DIM	9	dimming input, reducing the lamp-on-detection threshold; see Section 3.9 on page 27
BOOST	10	lamp current boost input (UBA2016A); see Section 3.10 on page 28
PH/EN	10	preheat frequency setting with enable/disable (UBA2015/UBA2015A); see Section 3.11 on page 31
GLHB	17	low-side half-bridge gate driver; see Section 3.18 on page 39
SHHB	18	hard switching regulation and protection input, ground of high-side driver, source of the dVdt supply; see Section 3.19 on page 40
FSHB	19	floating supply of the high-side driver; see Section 3.20 on page 40
GHHB	20	high-side half-bridge gate driver; see Section 3.21 on page 40

Table 4. Other function pins

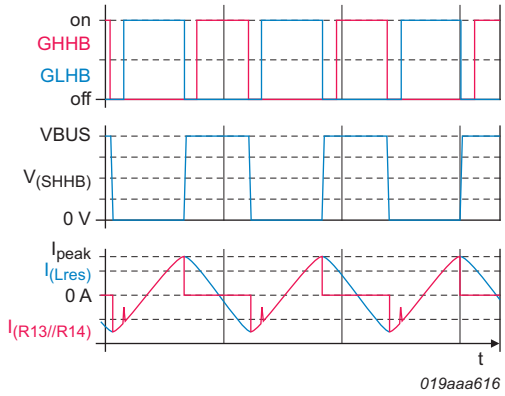
Symbol	Pin	Description
IREF	5	IC reference current; see Section 3.5 on page 24
GND	15	IC ground reference; see Section 3.16 on page 37
VDD	16	IC supply, gate drive supply, restart after re-lamp; see Section 3.17 on page 37

3.1 Pin SLHB: preheat current regulation, coil saturation protection

Refer to Figure 8.The half-bridge current is sensed by resistors R13 and R14 in parallel (R13//R14 = R_{SLHB}). During preheat, the half-bridge current is regulated by the half-bridge controller with a preheat threshold $V_{th(ph)(SLHB)}$ = 0.5 V. As a result, $V_{SLHB(peak)}$ = 500 mV.



a. Pin SLHB circuit diagram



b. Half-bridge current and voltage waveforms

Fig 8. Pin SLHB

The saturation protection is always active and it protects the circuit against:

- Coil saturation
- Overvoltage of the resonant tank and the lamp

The IC has a fixed ratio of five between the preheat level and the saturation voltage level. However, due to the internal bias current source of 8.5 µA the current ratio (saturation/preheat) of the half-bridge current can be increased by adding resistor Rx in series with pin SLHB.

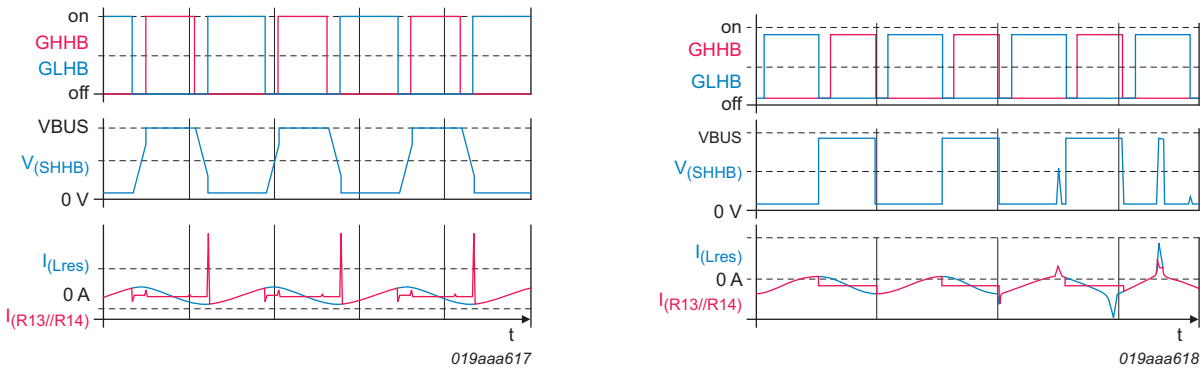
Once the component values of the half-bridge (HB) are known and therefore also the current during preheat and the saturation current of the HB inductor, the value for Rx can be calculated by Equation 1:

$$Rx = \frac{V_{th(ph)(SLHB)} \times I_{bias(SLHB)} + V_{th(ph)(SLHB)} \times I_{sat} - V_{th(sat)(SLHB)} \times I_{bias(SLHB)} - V_{th(sat)(SLHB)} \times I_{ph(peak)}}{I_{bias(SLHB)} \times (I_{sat} - I_{ph(peak)})} \quad (1)$$

$V_{th(ph)(SLHB)}$ = 0.5 V; $V_{th(sat)(SLHB)}$ = 2.5 V; $I_{bias(SLHB)}$ = 8.5 µA.

When Rx is known, the resistors R13 and R14 can be calculated by Equation 2:

$$R(13//14) = \frac{V_{th(ph)(SLHB)} - I_{bias(SLHB)} \times Rx}{I_{bias(SLHB)} + I_{ph(peak)}} \quad (2)$$



a. Hard switching

b. Coil saturation

Fig 9. Simulated current through low-side sense resistor (R13//R14)

The hard switching spikes on the SLHB are internally blanked with 300 ns (leading edge blanking) to prevent a false trigger of the coil saturation.

During preheat and ignition the saturation protection increases the HB operating frequency in order to reduce the HB inductor current and to allow the lamp to ignite. In preheat and ignition state the slow fault timer is used for saturation protection.

In burn state the saturation protection reacts very fast to detect lamp removal or broken lamp conditions.

3.2 Pin IFB: lamp current feedback, lamp-on detection, internal lamp current rectifier, overcurrent detection

Ballasts that run at the minimum operating frequency do not require a lamp current sense resistor and lamp-on detection. Pin IFB can be left open or shorted to ground. If no lamp-on is detected, the controller sweeps the frequency down. If the minimum switching frequency is reached the IC assumes that the lamp has ignited. The IC has an internal double-sided rectifier on pin IFB which has no voltage drop.

3.2.1 Lamp-on detection (LOD)

The LOD limits the visible flash when the ballast is switched on while the ballast control input is at a deep dim level.

After LOD (also known as ignition detection) is triggered the IC enters Burn state. The LOD threshold $V_{th(lod)(IFB)}$ is a function of the voltage on pin DIM. The relationship between the LOD threshold and the DIM voltage is shown in Figure 10.

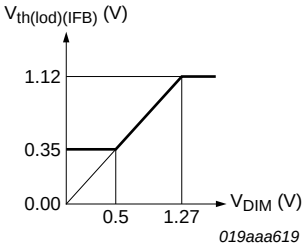


Fig 10. Lamp-on detection threshold

The LOD signal is internally filtered with a time-constant of approximately 100 μs; therefore the threshold must be compared to the average double-sided rectified voltage VIFB.

After ignition, the control loop regulates the frequency to the set point with the time-constant defined by the compensation network on pin CIFB. This ensures that sufficient ionization energy is transferred to the lamp.

3.2.2 Lamp current feedback

Ballasts that require only lamp current control without deep dimming, a single sense resistor is sufficient.

Applications that require deep dimming (below 10 %) are advised to use a non-linear sense circuit. The intention of the non-linear circuit is to guarantee a strong feedback signal for low lamp currents. This has two advantages during deep dimming:

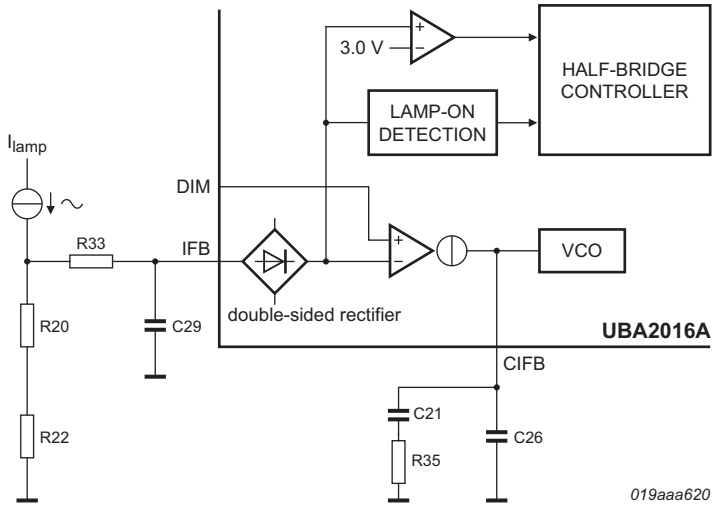
- The circuit is less sensitive to tolerances
- The circuit is less sensitive to low frequency ripples
- The minimum lamp current setting via input pin DIM is more accurate

Place resistor R33 and C29 close to the IC; see Figure 11b.

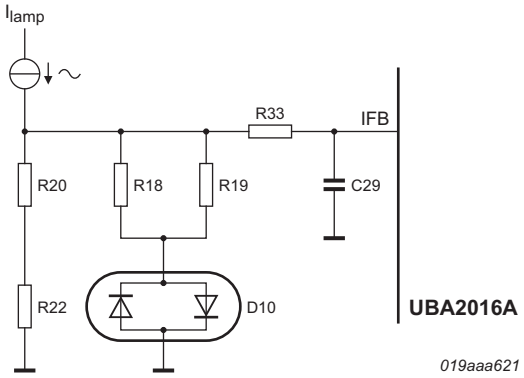
3.2.3 Overcurrent lamp protection

The IC enters Stop state when both of the following conditions are met:

- The peak of the absolute voltage at pin IFB exceeds $V_{th(ocd)(IFB)}$
- The IC is oscillating at f_{high}



a. Normal application with basic IC



b. Deep dimming

R18, R19, D10 not mounted.

Fig 11. Lamp current sense circuit and pin IFB

Typical values for lamps with nominal current of 300 mA:

Figure 11a: R20 = R22 = 2.4 Ω; R33 = 1.0 kΩ; C29 = 100 pF; R18 = R19 = reserved; D10 = reserved.

Figure 11b: R20 = R22 = 18 Ω; R18 = R19 = 2.7 Ω; R33 = 1.0 kΩ; C29 = 100 pF; D10 = PMBD7000.

3.2.3.1 Calculations for Figure 11a

$$I_{lamp(nom)(peak)} = I_{lamp(nom)} \times SQRT(2) = 424\ mA \quad (3)$$

After the double-sided rectifier the IFB signal is averaged by Equation 4.

$$I_{lamp(nom)(avg)} = I_{lamp(nom)(peak)} \times (2/\pi) = 270\ mA \quad (4)$$

The internal regulation voltage $V_{reg(IFB)}$ = 1.27 V when pin DIM voltage is not pulled down by the application.

The value for R20 plus R22 is calculated by Equation 5.

$$R20 + R22 = \frac{V_{reg(IFB)}}{I_{lamp(nom)(avg)}} = 4.7\,\Omega \quad (5)$$

Therefore R20 = R22 = 2.35 Ω.

3.2.3.2 Calculations for Figure 11b

The value of the parallel resistance of R18 and R19 is calculated by Equation 6.

$$R(\mathrm{R18//R19}) = \frac{V_{reg(IFB)} - V_{f(avg)}}{I_{lamp(nom)(avg)}} = 1.37\,\Omega \quad (6)$$

Because the average forward voltage of the diode increases as a function of the current through the diode, the $V_{f(avg)} = V_f \times 1.5$ (based on measurements).

The dimming target of the RMS lamp current is 2 % of nominal. $I_{lamp(dim)(rms)}$ = 6.0 mA.

The average lamp dimming current is calculated by Equation 7.

$$I_{lamp(dim)(avg)} = I_{lamp(dim)(rms)} \times SQRT(2) \times \frac{2}{\pi} = 5.4\,mA \quad (7)$$

Pin IFB voltage level at deep dimming must be 150 mV or higher. The reason for this is the accuracy of the internal double-sided rectifier.

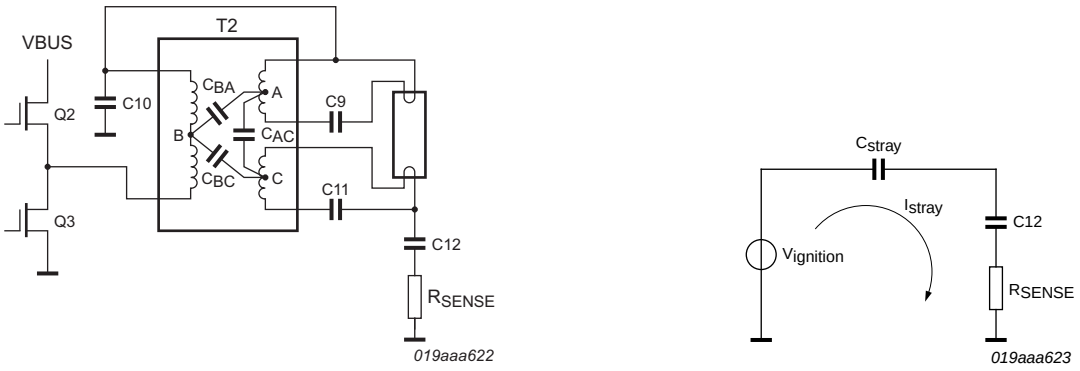
The value of the series resistance of R20 plus R21 is calculated by Equation 8.

$$R(20 + 22) = \frac{V_{reg(IFB)(dim)}}{I_{lamp(dim)(avg)}} = 28\,\Omega \quad (8)$$

Where $V_{reg(IFB)(dim)}$ = 150 mV, therefore R20 = R22 = 14 Ω.

3.2.3.3 Lamp at end-of-life and deep dimming sense circuit

The IC tries to ignite the broken lamp, until the fault timer expires, while the operating frequency is controlled by the voltage regulation via pin VFB. Because of the high voltage across the resonant capacitor and the half-bridge transformer, a current flows through the “lamp current-sense circuit” due to the parasitic capacitances inside the half-bridge transformer. Care must be taken to ensure that the lamp-on detection is not triggered. Therefore the values of R20 and R22 in Figure 11b (deep dimming) must not be too high; see Figure 12.



a. Positions of stray capacitances in the half-bridge transformer

b. Simplified model showing the stray current

Fig 12. Stray capacitances of a half-bridge transformer for inductive topology

R_{sense} = R20 + R22.

The stray capacitance is the combination of all inter-winding capacitances (Equation 9).

$$C_{stray} = C_{BC} \equiv (C_{BA} + C_{AC}) \quad (9)$$

C12 is much larger then C_{stray}, therefore C12 can be ignored. The stray current is calculated by Equation 10.

$$I_{stray} = V_{ignition} \times (2 \times \pi \times f_{ignition} \times C_{stray}) \quad (10)$$

The average stray current is calculated by Equation 11.

$$I_{stray(avg)} = 4 \times V_{ignition(peak)} \times f_{ignition} \times C_{stray} \quad (11)$$

A design requirement is applied to prevent false LOD triggering in deep dimming non-linear current sense circuits as shown in Equation 12.

$$I_{stray(avg)} \times R_{sense} < 150\ mV \quad (12)$$

which is equal to Equation 13.

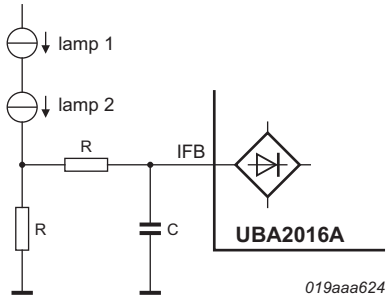
$$4 \times V_{ignition(peak)} \times f_{ignition} \times C_{stray} \times R_{sense} < 150\ mV \quad (13)$$

Some realistic values are:

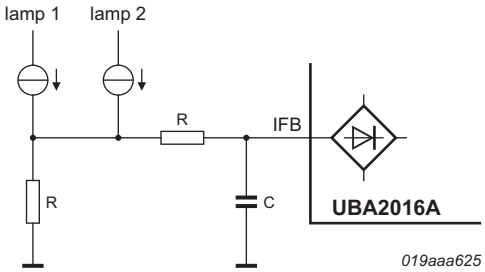
$V_{ignition(peak)}$ = 1200 V; $f_{ignition}$ = 60 kHz; C_{stray} = 15 pF → R_{sense} < 35 Ω.

3.2.3.4 Multiple lamp current sense

The lamp current sense circuit for multiple lamps is very similar to the single lamp application; see Figure 13.



a. Lamps in series



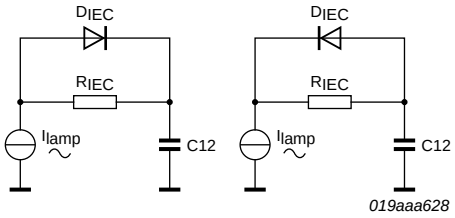
b. Lamps in parallel

Fig 13. Lamp current sense for multiple lamps

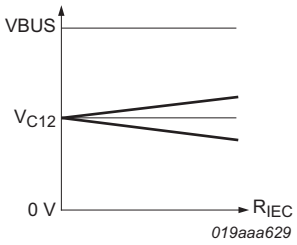
3.3 Pin EOL: lamp end-of-life detection

The voltage on pin EOL is fed to the internal window comparator. The window lower limit equals the FBPFC voltage and the upper limit is equal to twice the FBPFC voltage.

Asymmetric aging effects of the lamp (also known as the IEC rectifying and asymmetric pulse) can be sensed by sensing the voltage on DC blocking capacitor C12. The sensitivity and DC shift can be adjusted independently due to the internal current source $I_{bias(EOL)}$; see Figure 14.



a. Lamp end-of-life IEC test circuit (the diode can be connected in either polarity)



b. Relationship between DC blocking capacitor voltage and asymmetric power consumption

Fig 14. Asymmetrical lamp end-of-life IEC test circuit and DC blocking voltage

The power dissipated in the test resistor R_{IEC} must be below the IEC requirement of $P_{EOL(max)}$ = 7.5 W for T5 lamps and $P_{EOL(max)}$ = 5.0 W for T4 lamps. R_{IEC} has to be determined by practical measurement: R_{IEC} is increased until the maximum power is reached.

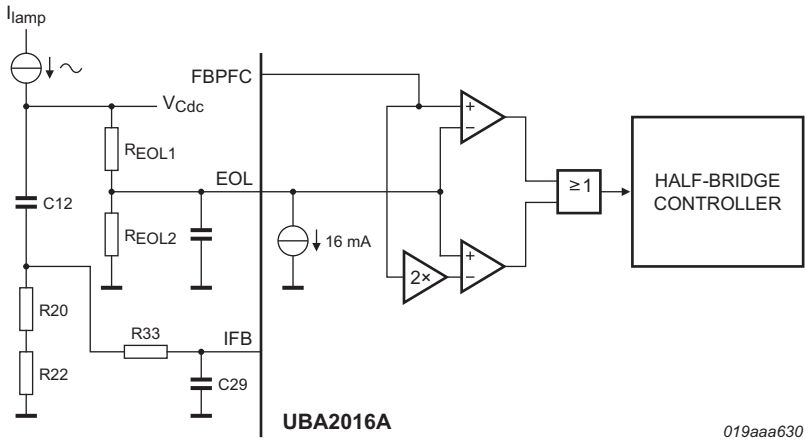
The voltage on C12 is calculated by Equation 14.

$$V_{C12} = \frac{VBUS}{2} \pm \frac{P_{eol}}{I_{lamp}} \quad (14)$$

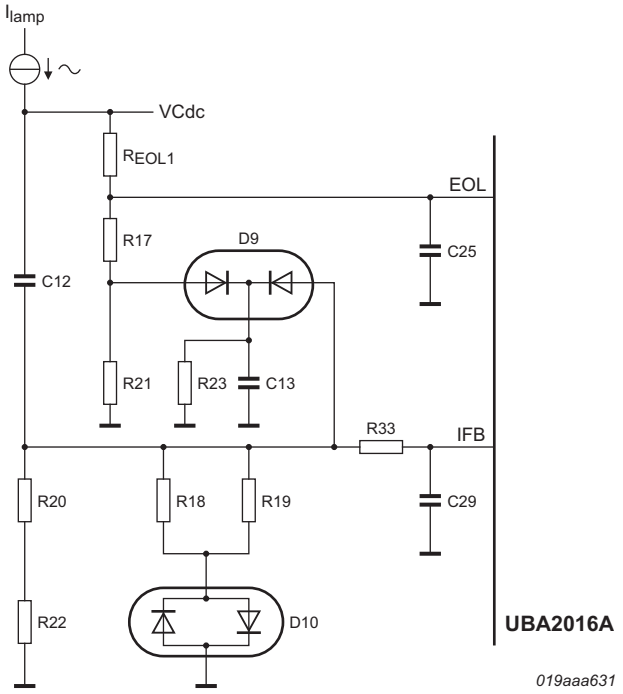
The voltage on C12 will shift as a function of the power dissipated in R_{IEC}.

The maximum EOL power $P_{EOL(max)}$ is an IEC requirement. $P_{EOL(max)}$ for T5 is 7.5 W and for T4 it is 5 W. Currently there are no IEC requirements for T8 lamps, however it is recommended to use a $P_{EOL(max)}$ of 10 W ~ 12.5 W for T8 lamps. The lamp current I_{lamp}

depends on the lamp type. The voltage shift of the DC blocking capacitor due to asymmetrical aging can fit into the IC's end-of-life window by the application resistor divider. The resistor divider consists of R_{EOL1} (R6 and R7 in Figure 3 on page 7) and R_{EOL2}.



a. Fixed output and dimming down to 10 %



b. Deep dimming <10 %

Fig 15. Pin EOL application with DC blocking capacitor C12 sensing

In deep dimming application, the voltage on the DC blocking capacitor shifts if a DC current through the lamp is used for cancelling striation. A compensation circuit (D9, R23, C13, R21) shown in Figure 15b can be used when V_{C12} rises when dimming is below 10 % of the nominal lamp current.

3.3.1 Calculation of the resistor divider R_{EOL1} and R_{EOL2}

See Figure 15a.

The voltage at pin EOL is shown in Equation 15.

$$V_{EOL} = \frac{V_{C12} \times R_{EOL2} - I_{bias(EOL)} \times R_{EOL1} \times R_{EOL2}}{R_{EOL1} + R_{EOL2}} \quad (15)$$

Where $I_{bias(EOL)}$ = 16 μA.

The EOL window threshold voltages are: $V_{th(low)(EOL)} = 1 \times V_{FBPFC}$, $V_{th(high)(EOL)} = 2 \times V_{FBPFC}$. Under normal operation the V_{FBPFC} voltage is 1.27 V as shown in Equation 16.

$$V_{EOL(window)(range)} = (V_{th(high)(EOL)} - V_{th(low)(EOL)}) = V_{FBPFC} = 1.27\ V \quad (16)$$

The EOL window centre voltage is calculated by Equation 17.

$$V_{EOL(window)(center)} = \frac{V_{th(high)(EOL)} + V_{th(low)(EOL)}}{2} = 1.91\ V \quad (17)$$

The allowed voltage shift on the DC block capacitor determines the ratio between R_{EOL1} and R_{EOL2} calculated by Equation 18.

$$\frac{R_{EOL1}}{R_{EOL2}} = \frac{2 \times P_{EOL} - V_{EOL(window)(range)} \times I_{lamp}}{V_{EOL(window)(range)} \times I_{lamp}} \quad (18)$$

Where P_{EOL} is the maximum power dissipated asymmetrically.

The absolute values for R_{EOL1} and R_{EOL2} center the voltage in the EOL window, calculated by Equation 19 and Equation 20.

$$R_{EOL1} = \frac{\frac{V_{EOL(window)(range)} \times I_{lamp} \times VBUS}{2 - 2 \times V_{EOL(window)(center)}}}{V_{EOL(window)(range)} \times I_{lamp} \times I_{bias(EOL)}} \quad (19)$$

$$R_{EOL2} = \frac{\frac{V_{EOL(window)(range)} \times I_{lamp} \times VBUS}{2 - 2 \times V_{EOL(window)(center)}}}{V_{EOL(window)(range)} \times I_{lamp} - 2 \times P_{EOL} \times I_{bias(EOL)}} \quad (20)$$

Table 5. Calculated values for R_{EOL1} and R_{EOL2} for pin EOL application

Lamp	VBUS (V)	P_{EOL} (W)	I_{lamp} (mA)	R_{EOL1} (MΩ)	R_{EOL2} (kΩ)
T5HE14W; T5HE21W; T5HE28W; T5HE35W	432	7.5	170	7.99	176
T5HO24W			300	10.4	411
T5HO39W			340	10.7	485
T5HO49W			260	9.90	338
T5HO54W			460	11.5	711
T5HO80W			555	11.8	896

Use 1 % resistors such as the MRS type from Vishay BC Components for the EOL divider. Note that also the PFC output voltage must have 1 % accuracy because the voltage on the DC blocking capacitor is 0.5 times the bus voltage.

3.4 Pin VFB: lamp voltage feedback, overvoltage detection, open/short protection

The advantage of lamp voltage feedback is that it limits voltage stress on the half-bridge components such as NMOST, inductor and capacitors. The lamp voltage feedback signal can be derived from the LC tank voltage. The IC has a separate pin for voltage feedback, this is advantageous in multi-lamp applications because the IC will regulate on the maximum voltage of both lamps.

When a lamp is removed or breaks in burn state, an immediate shutdown is activated when the shutdown threshold on pin VFB is reached. As a result, the excessive voltage is only briefly on the half-bridge resonant node.

3.4.1 Lamp voltage regulation

In preheat state and ignition state, when the VFB voltage is above $V_{th(ov)(VFB)}$ = 2.5 V, the switching frequency is increased (lowering the voltage on the resonant tank) and the fault timer is started. This protects the ballast under no lamp conditions. The IC will try again to ignite the lamp and if after the second time the lamp still does not ignite the IC enters the standby state.

3.4.2 Overvoltage protection

In any state when the VFB voltage is above $V_{th(ovextra)(VFB)}$ = 3.5 V, the controller enters Stop state immediately. This mechanism prevents excessive component stress when the lamp is removed while the actual switching frequency is below the unloaded resonant frequency.

3.4.3 EOL protection symmetrical lamp aging

Fluorescent lamps age over time. As a result, the lamp voltage can increase. The VFB voltage is compared with threshold $V_{th(oveol)(VFB)}$. If the VFB voltage exceeds this threshold, the slow fault timer is started. The threshold is increased when the lamp is dimmed because the lamp voltage rises when the lamp current decreases. The threshold levels are shown in Table 6.

Table 6. Threshold levels at different dimming voltages

V_{DIM} (V)	$V_{th(oveol)(VFB)}$ (V)
1.27 (pin DIM open)	0.88
1.0	1.0
0.5	1.23

3.4.4 Open/short protection

When the VFB voltage is below $V_{th(osp)(VFB)}$ = 80 mV, the switching frequency is increased and the fault timer is started. Pin VFB is pulled LOW by $I_{bias(VFB)}$ in case the pin is open.

3.4.5 Circuit diagram

Refer to Figure 16. A capacitive divider reduces the peak-to-peak voltage to below 300 V and the diode clamps the signal to ground. The feedback signal can be tuned with the resistor divider R10 and R11. A conventional series-resonant application is shown but this arrangement also applies to inductive mode series-resonant applications.

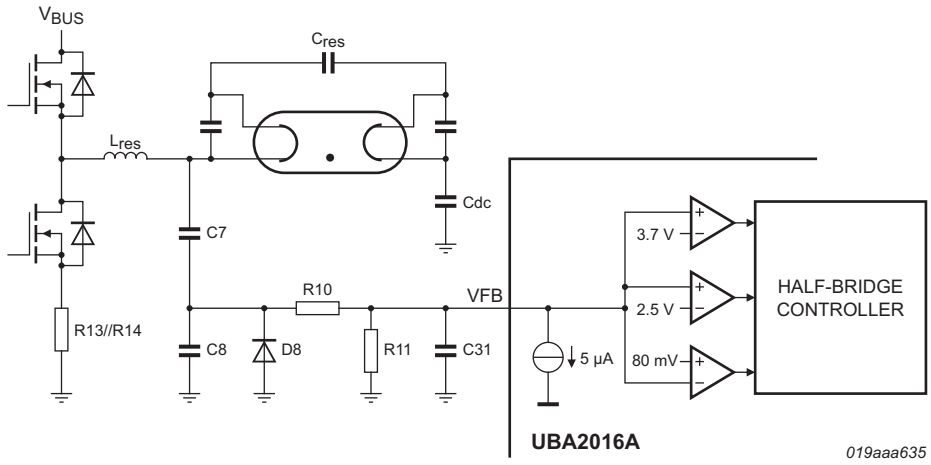


Fig 16. Typical pin VFB application

Typical values for a pin VFB application are:

R10 = 100 kΩ; R11 = 5.6 kΩ; C7 = 100 pF; C8 = 1.5 nF C31 = 10 nF; D8 = BAS101S.

3.4.5.1 Calculation of pin VFB components

The value of C7 is fixed: C7 = 100 pF. The value of C8 is calculated by Equation 21.

$$C8 = \left(C7 \times \frac{1 - V_R \times \frac{1 - margin}{2 \times V_{max} - VBUS}}{V_R \times (1 - margin)} \right) \times 2 \times V_{max} - VBUS \quad (21)$$

The value of R10 is determined by the time constant t = C8 × (R10 + R11) and must be about 2 ms.

Where margin = 0.3 and is a constant. V_{max} is the worst case ignition voltage. V_R is the maximum reverse voltage of the clamp diode. A diode with a V_R of 300 V or higher requires sufficient voltage at startup to satisfy $V_{th(osp)(VFB)}$. The value of R11 is calculated by Equation 22.

$$R11 = 2 \times R10 \times \frac{V_{reg}}{(2 \times V_{max} - VBUS) \times C7} \times \frac{C7 + C8}{1 - 2 \times \frac{V_{reg}}{(2 \times V_{max} - VBUS) \times C7} \times (C7 + C8)} \quad (22)$$

Capacitor C31 filters noise on the VFB PCB track. The value of C31 must not be too high to enable the IC to react quickly when the lamp is removed if the switching frequency is near the resonant frequency of the LC tank that has a high Q factor (inductive series resonant topology). A time-constant of 100 ns is advised. The value of C31 is calculated by $C31 \times R11 = 100\ ns$.

3.5 Pin IREF: IC reference current

Pin IREF must be connected via a resistor R34 of 33 kΩ to ground.

3.6 Pin CIFB: input for the internal VCO, time-constant of the lamp current control loop, ignition frequency ramp-down speed after preheat

3.6.1 VCO input

When pin CIFB is 0 V the half-bridge switching frequency is at f_{high}.

When pin CIFB is at $V_{high(CIFB)}$ = 3.0 V the half-bridge switching frequency is at f_{low}.

3.6.2 Lamp current control

The half-bridge frequency is determined by the average voltage on pin IFB. If pin IFB is not used, the switching frequency in Burn state is f_{low}.

Since pin CIFB is the output of the error amplifier, the speed of the control loop is determined by the capacitance on pin CIFB.

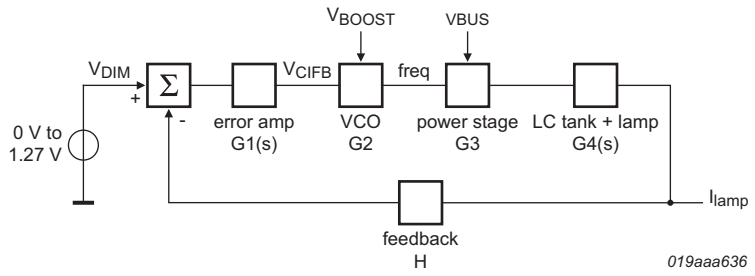
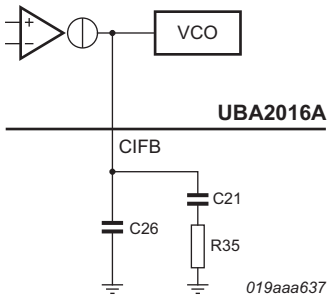
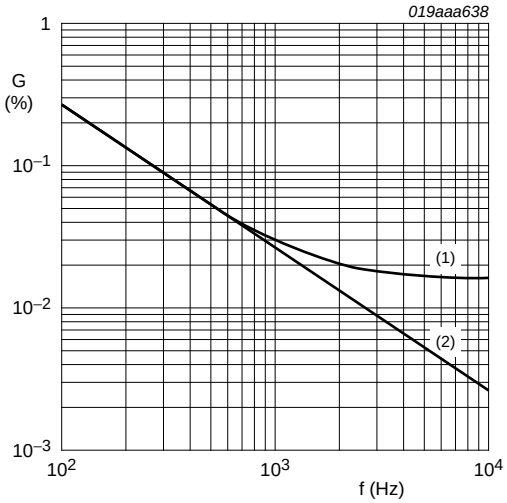


Fig 17. Small signal block diagram of the lamp current control loop

Figure 18a shows the transfer of the error amplifier with the CIFB compensation network. This transfer is equal to G1(s) in Figure 17.



a. Pin CIFB application



b. Small signal transfer (gain versus frequency)

(1) C26, C21 and R35.

(2) C26 (C21 and R35 not mounted).

Fig 18. Frequency response of error amplifier plus CIFB network

Typical values for the CIFB network are:

Non-dimmable ballasts: C26 = 100 nF; C21 = reserved; R35 = reserved;

Dimmable ballasts: C26 = 3.3 nF; C21 = 100 nF; R35 = 1 kΩ.

In cases where lamp currents are low (deep dimming), the lamp's discharge column is close to extinguishing, in this situation the time-constant of the lamp is small. The control loop has to be fast enough to prevent the lamp from extinguishing. Therefore, for a dimmable ballast, C21 and R35 must be added to increase the gain and speed of the control loop in order to react faster than the time-constant of the lamp.

3.7 Pin CF: timing capacitor of oscillator

The oscillator frequency is twice the operating frequency of the half-bridge. To guarantee a 50 % duty cycle, the half-bridge operates at half the oscillator frequency. The frequency range is set by capacitor C27 in the internal relaxation oscillator. The value of C27 is calculated by Equation 23.

$$C27 = \frac{I_{cf}}{2 \times f_{low} \times V_{th(cf)}} \quad (23)$$

Where I_{cf} = 43 μA; $V_{th(cf)}$ = 2.5 V.

The maximum switching frequency (f_{high}) is set by a fixed ratio: $f_{high} = f_{low} \times 2.4$.

A typical value for C27 is 220 pF, this will give a f_{low} of 39 kHz and hence an f_{high} of 94 kHz; see Figure 19.

If C27 is a ceramic capacitor, it is advisable to only use those that have an NP0 or C0G dielectric, for high accuracy and temperature independency. When no lamp current control is used it is advisable to use a 1 % capacitor for an accurate switching frequency.

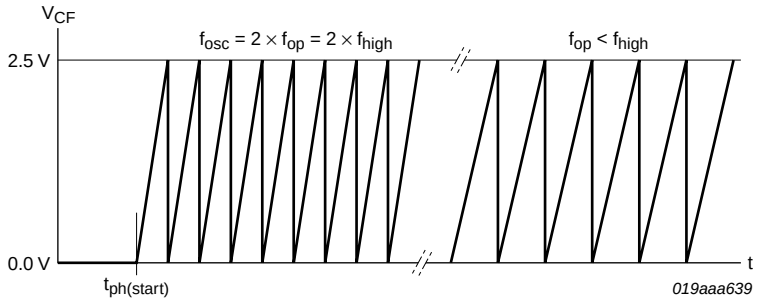


Fig 19. Voltage on pin CF

The capacitor C27 is charged by a current source until the threshold of 2.5 V is reached; at this point C27 is discharged after approximately 300 ns. The IC regulates the amount of charge current and therefore the switching frequency.

3.8 Pin CPT: preheat timer, fault timer, open/short protection

Preheat and fault time duration is set by the capacitor on pin CPT whose value is calculated by Equation 24.

$$C30 = \frac{t_{ph}}{CPT_{constant}} \quad (24)$$

Where $CPT_{constant} = 10 \times 10^6$.

A typical value for C30 is 100 nF, this gives a preheat time $t_{to(ph)}$ of 1000 ms.

When C30 is a ceramic capacitor, it is advisable to use those that have an X7R dielectric. The X7R capacitance decreases when a DC voltage is applied, therefore the voltage rating must be 50 V even though a lower voltage is applied.

3.8.1 Preheat timer

The preheat timer counts 8 times to charge capacitor C30 to 3.7 V with a current of 5.4 μA. The discharge current (which is equal to the charge current) is applied until the voltage on C30 reaches 1.0 V; see Figure 20.

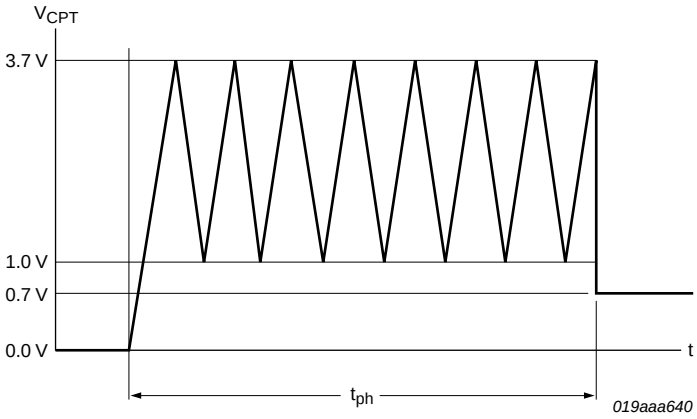


Fig 20. Voltage on pin CPT during preheat

3.8.1.1 Fault timer

The fault timer provides a delay between fault detection and shutdown. The fault time duration is one fifth of the preheat time.
Since both timers use the same pin, the fault timer takes priority over the preheat timer. The preheat timer restarts after a fault has cleared.

3.8.1.2 Open/short protection

When the CPT voltage is below $V_{th(scp)(CPT)}$ = 120 mV, the controller does not sweep the frequency down to the preheat frequency but continues switching at f_{high}. This prevents endless preheating if a short or open circuit production fault occurs on this pin.

When the CPT voltage is pulled below $V_{th(scp)(CPT)}$ while the IC is in any oscillating state, the controller increases the switching frequency to f_{high} with a time-constant of approximately 7 ms. Pin CIFB can be shorted to ground in case a shorter time-constant is needed.

The open/short protection on pin CPT allows an (optional) external protection circuit to switch the operating frequency to f_{high}. At f_{high} the power in the LC tank is minimal and the voltage stress on the half-bridge components is minimal.

3.9 Pin DIM: reduces lamp current control set point, reduces the lamp-on-detection threshold

3.9.1 Lamp current regulation

The controller regulates the frequency such that the average voltage on pin IFB during Burn state equals the DC voltage on pin DIM.

The lamp current regulation level is equal to the voltage at pin DIM. Internally the maximum regulation level is clamped to $V_{reg(IFB)}$ = 1.27 V. During the startup cycle (Preheat and Ignition state) the minimum regulation level is clamped to $V_{reg(start)(IFB)}$ = 500 mV. In Normal state the minimum regulation level is 0 V, however it is advisable to design the minimum level to be 150 mV for better accuracy and also to prevent detection of false ignition (lamp-on detection) via pin IFB.

3.9.1.1 Lamp-on detection

The lamp-on detection limits the visible flash when the ballast is switched on while the ballast control input is at a deep dim level.

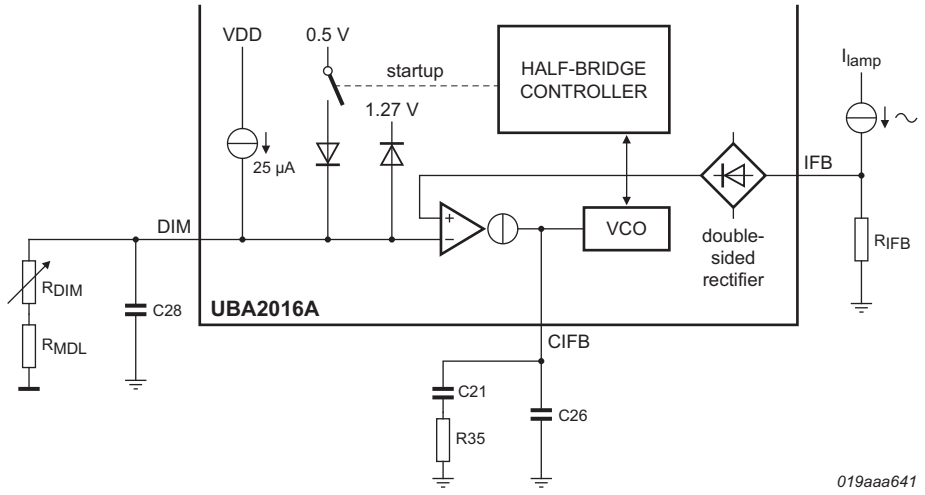


Fig 21. Pin DIM application

If no dimming is required, pin DIM must be connected to ground via a capacitor C28 = 10 nF. The internal current source $I_{bias(DIM)}$ will charge C28 to the maximum voltage; see Figure 21.

If dimming is required, the voltage on pin DIM must be decreased to reduce the lamp current. A resistor or a voltage source that can sink at least 25 µA of current is sufficient.

R_{DIM} in Figure 21 is used to set the voltage, R_{MDL} is used to set an accurate minimum dim level.

3.10 Pin BOOST: increase lamp current control set point

The UBA2016A has a boost function that is intended to shorten the run-up time of the lamp. This is mainly used for amalgam lamps or outdoor applications; see Figure 22.

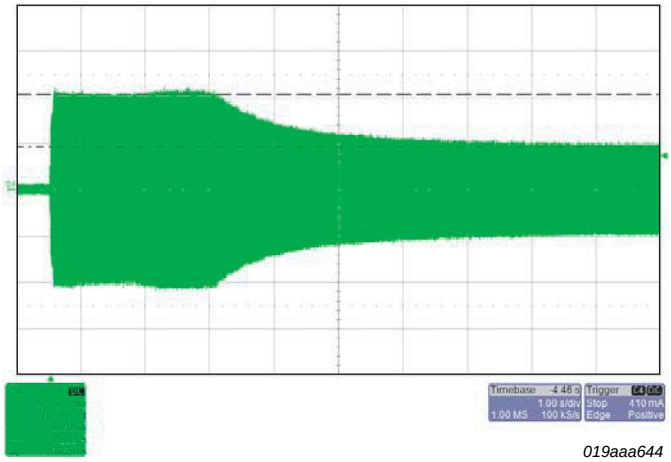
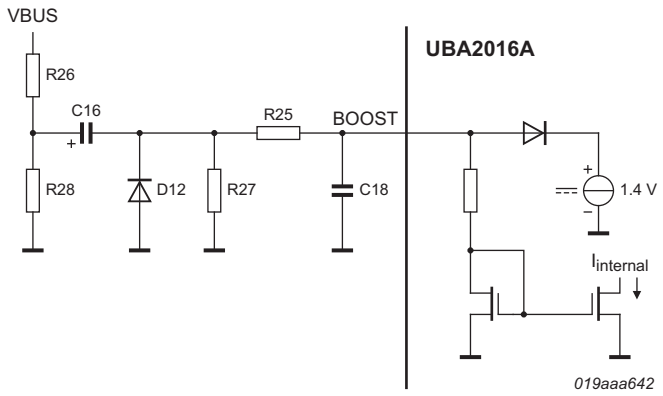


Fig 22. Boost function of the lamp current at startup

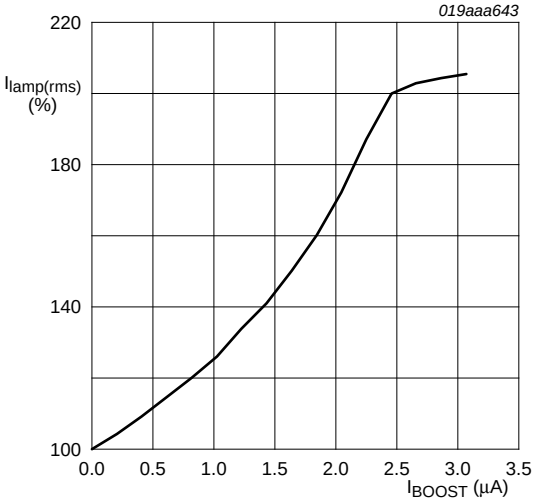
The lamp current is increased as a function of the current that flows into the BOOST pin. Figure 23b shows the measured data of the RMS lamp current versus the BOOST pin current; in this case a non-linear lamp current sense circuit Figure 11b is used.

During the boost time, the minimum operating frequency f_{low} is reduced to 50 %. The BOOST pin current increases the light output that is more than nominal; this is different to applying more voltage to the DIM input. Control via pin DIM only reduces the current flow which limits the power.

When not needed, pin BOOST must be connected to ground or consider using the UBA2015 which has a fixed frequency preheat function instead of the boost function.



a. Pin BOOST components



b. Pin BOOST current as a function of lamp current

Fig 23. BOOST application

Refer to Figure 23a. Typical values for the boost network are:

R25 = 10 kΩ; R26 = 2.2 MΩ; R27 = 470 kΩ; R28 = 47 kΩ; C16 = 10 µF; C18 = 10 nF; D12 = PMBD914.

The boost time is equal to the discharge time of capacitor C16 minus the preheat time; R27 is in the circuit to discharge C16 completely. C18 must be placed to make the input less sensitive to noise.

The boost voltage must not exceed the limiting values of +2.5 V:

Calculate R26, R28.

Pin BOOST current must not exceed 100 µA when D12 is in forward mode:

Calculate R25: 10 kΩ is sufficient in most cases.

The boost function must be supported by the half-bridge circuit; therefore the following two rules apply:

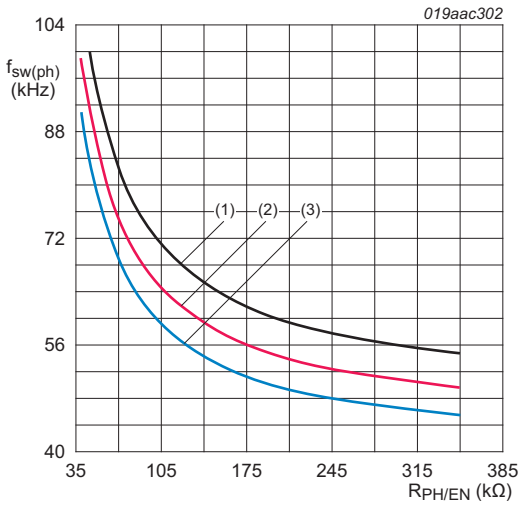
$$VBUS > 8 \times f_{bst} \times L_{res} \times SQRT(3) \quad (25)$$

$$f_{low(bst)} > \frac{1}{pi \times SQRT \times L_{res} \times Cdc} \quad (26)$$

The first rule (Equation 25) ensures that the lamp current can be reached; the second rule (Equation 26)ensures that the half-bridge switching node is not operated in capacitive mode.

3.11 PH/EN: fixed frequency preheat, enable/disable, burn state indication output

The fixed frequency preheat is set by a resistor from pin PH/EN to ground in the UBA2015 and UBA2015A. The preheat frequency is shown as a function of $R_{PH/EN}$ for CF = 180 pF, 200 pF and 220 pF.



(1) CF = 180 pF.
(2) CF = 200 pF.
(3) CF = 220 pF.

Fig 24. Preheat frequency as a function of $R_{PH/EN}$

The controller can be disabled by pulling pin PH/EN below 250 mV with a transistor. This could be useful for power management or additional protection that needs a fast shutdown.

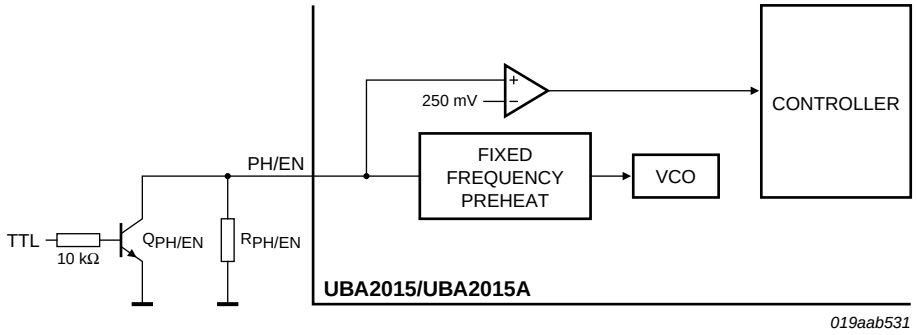


Fig 25. Pin PH/EN application example with enable/disable transistor

Pin PH/EN indicates when the burn state is entered. This function can be used to operate a switch in the half-bridge circuit to change the LC tank between preheat and burn state.

In preheat and ignition state the output voltage is 1.84 V. In burn state the output voltage is 1.27 V.

3.12 Pin FBPFC: PFC voltage feedback, overvoltage protection, overcurrent protection, open/short protection

The brownout functionality is assigned to pin COMPPFC; see Section 3.13.

3.12.1 PFC voltage feedback

The PFC controller is always active when the half-bridge is active. The half-bridge switching frequency is kept at $f_{high(HB)}$ until the voltage on pin FBPFC is above $V_{th(VPFCok)(FBPFC)}$ = 1.0 V.

The voltage on pin FBPFC connects to the error amplifier of the PFC control loop. Pin FBPFC is connected to the PFC output voltage VBUS and it is compared with an internal voltage of $V_{reg(FBPFC)}$ = 1.27 V.

3.12.1.1 Overvoltage protection (0 V)

The FBPFC voltage is compared with an internal voltage of $V_{th(ov)(FBPFC)}$ = 1.39 V, internally, leading edge blanking is applied at the rise of GPFC. If 0 V occurs, GPFC is immediately set to LOW and kept LOW if VFBPFC is below 1.39 V.

3.12.1.2 Overcurrent protection

The PFC current sense is connected to pin FBPFC via a diode to prevent damage to the PFC NMOST if coil saturation/overcurrent occurs.

Note that the negative temperature coefficient of the diode's forward voltage (almost) compensates for the maximum flux density (B_{max}) of the PFC inductor. Typically a diode such as PMBD914 or 1N4148 is preferred. Do not use a Schottky diode because of its high leakage current properties.

3.12.1.3 Open/Short Protection (OSP)

When the FBPFC voltage is below $V_{th(osp)(FBPFC)}$ = 250 mV the PFC gate drive is disabled.

The internal bias current sink of $I_{bias(FBPFC)}$ = 5 μA ensures that VFBPFC is LOW if the pin is left open.

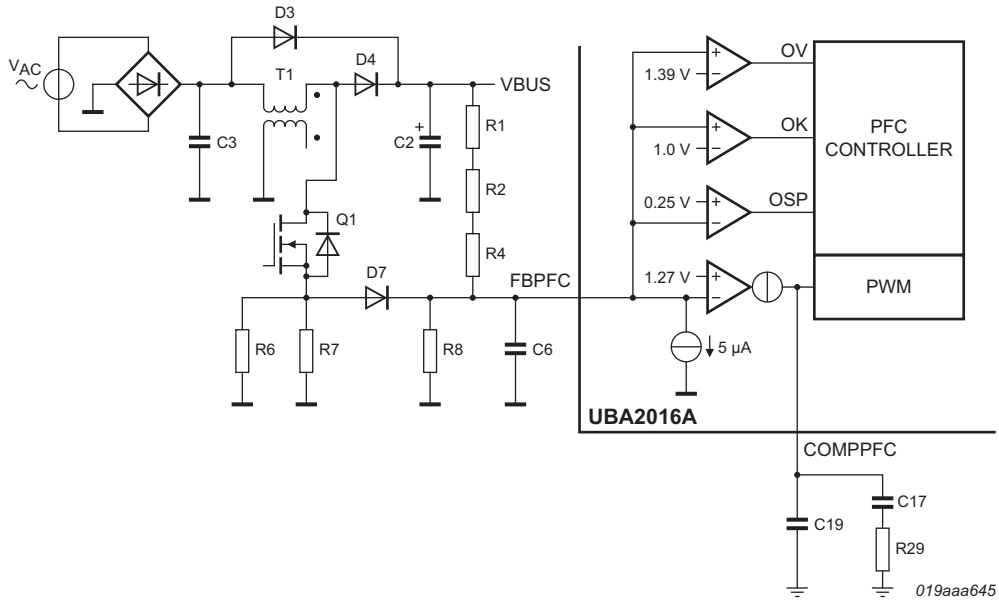


Fig 26. Pin FBPFC and COMPPFC application

Typical values for the pin applications: C6 = 47 pF; R8 = 3.3 kΩ.

The time-constant of capacitor C6 and R8 must not exceed the leading edge blanking time of 300 ns: $t_{leb} = C6 \times R8 < 330\ ns$.

To prevent noise being injected into the feedback loop, ensure R8 ≤ 3.3 kΩ.

Calculate the sum of R1, R2, and R4 for the correct output voltage using Equation 27:

$$(R1 + R2 + R4) = R8 \times \frac{(VBUS - 1.27)}{1.27} \quad (27)$$

Use 1 % resistors for R1, R2, R4 and R8 and the same type (temperature coefficient) for an accurate bus voltage and accurate voltage on the DC blocking capacitor. The voltage of the DC blocking capacitor is used for lamp end-of-life detection.

Calculate the value of R6 and R7 in parallel for the correct PFC overcurrent protection using Equation 28.

$$R(6//7) = \frac{1.27 + 0.6}{I_{PFC(peak)} \times 1.1} \quad (28)$$

3.12.1.4 Layout rules

Place capacitor C6 close to transistor Q1 to keep the switching noise local to Q1.

3.13 Pin COMPPFC: PFC voltage control loop compensation network, input of on-time modulator

A pin COMPPFC application is shown in Figure 26. The typical values are:

C19 = 100 nF; C17 = 470 nF; R29 = 82 kΩ.

3.13.1 Compensation network

The compensation network should be designed to have unity gain in the PFC control loop at 20 Hz. It is a trade-off between Power Factor and transient behavior. A lower bandwidth leads to a better Power Factor but the transient behavior is less. A higher bandwidth leads to a better transient behavior but the Power Factor is less.

The components C17 and R29 are added to have maximum phase margin at the unity gain frequency.

3.13.1.1 On-time modulator input

The voltage on pin COMPPFC determines the on-time of the PFC gate drive signal. A low voltage results in a low on-time, a high voltage (equal to $V_{high(COMPPFC)}$ = 3.0 V) results in a maximum on-time of 28 μs.

3.13.1.2 Brownout undervoltage

If a brownout occurs and undervoltage, the COMPPFC voltage increases and therefore also the on-time. However, when the COMPPFC voltage reaches 3.0 V the on-time does not increase; furthermore a signal is sent to the lamp controller to reduce the lamp power by increasing the half-bridge switching frequency.

3.14 Pin AUXPFC: demagnetization detection, THD wave shaper, open pin protection

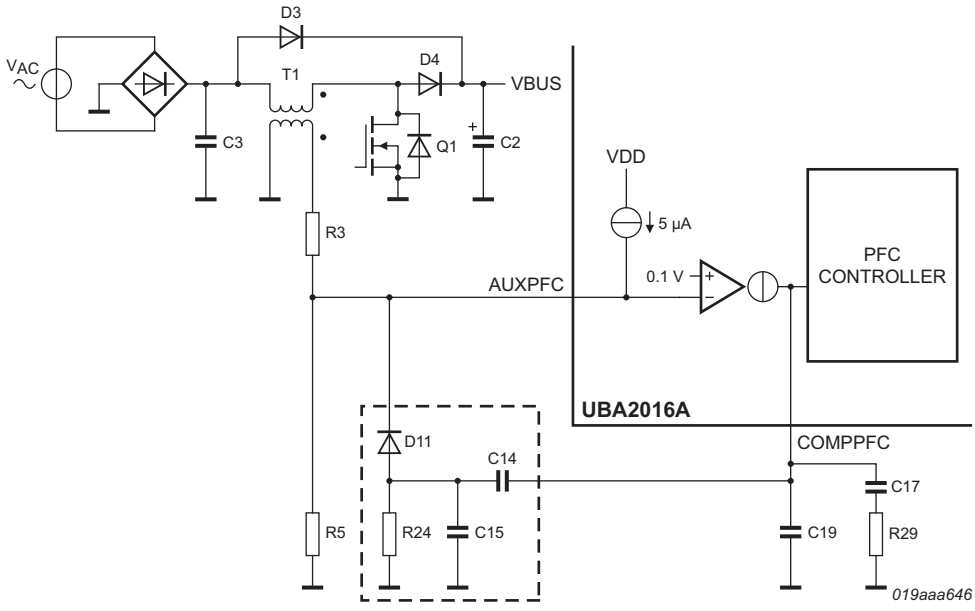


Fig 27. Basic circuit diagram of pin AUXPFC

Typical values of the application shown in Figure 27:

R3 = 10 kΩ; R5 = reserved; R24 = 10 kΩ; D11 = PMBD914; C15 = 100 nF; C14 = 4.7 nF.

3.14.1 PFC auxiliary winding

To protect the IC against a too high voltage, for example during lightning surge events, it is recommended to add a 10 kΩ series resistor (R3) to AUXPFC.

The number of turns of the auxiliary winding on the PFC coil and the maximum voltage across the PFC inductor can be calculated.

The PFC output voltage at overvoltage protection $VBUS_{(ov)}$ determines the maximum voltage across the PFC primary winding as shown in Equation 29.

$$VBUS_{(ov)} = \frac{VBUS \times V_{th(ov)(FBPFC)}}{V_{th(reg)(FBPFC)}} = VBUS \times 1.1 \quad (29)$$

It is important to maintain demagnetization detection even at low ringing amplitudes. The voltage at pin AUXPFC should be set as high as possible, while taking into account its absolute maximum rating of ±9 V ($V_{AUXPFC(max)}$) on the pin, with a safety margin of −10 %.

The number of secondary windings is calculated by Equation 30.

$$Np = \frac{Ns \times VBUS_{(ov)}}{V_{AUXPFC(max)} \times 0.9} = \frac{Ns \times VBUS_{(ov)}}{0.81} \quad (30)$$

When using a PFC coil with a higher number of auxiliary turns, a resistor voltage divider (using R5) must be placed between the auxiliary winding and pin AUXPFC to keep the voltages on pin AUXPFC within limits. The total resistive value of the divider should be small to prevent pickup of noise.

3.14.1.1 THD wave shaper circuit

To reach a THD performance better then 25 % THD, the on-time of the PFC must be modulated. With the wave shaper circuit a THD < 8 % can be reached over a large input voltage range. The modulation increases the on-time when the absolute mains voltage decreases. The AUXPFC signal can be used for this. After peak rectifying and filtering, the signal is injected into pin COMPPFC capacitor.

A short description of the THD wave shaper circuit:

- D11 rectifies the negative peak of the V_{AUXPFC};
- R24 and C15 buffer the rectified signal with the correct time-constant
- C14 injects the compensation current into pin COMPPFC; the capacitance determines the amount of compensation

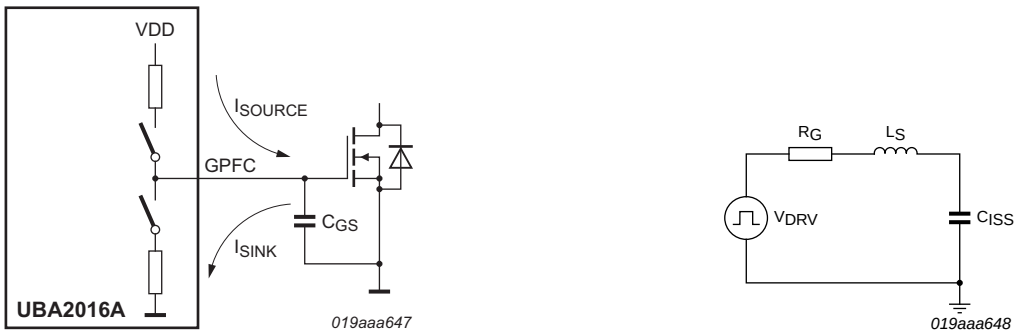
The time-constant of R24 and C15 is calculated by: $R24 \times C15 > 1\ ms$.

The best value for C14 must be determined by measurement.

3.15 Pin GPFC: PFC gate driver

There is no need for a series resistor in the gate drive track.

The strong switch-off capability ensures that the external MOSFETs are not switched on due to the current through the gate-drain capacitance of the external MOSFET.



a. Sink and source currents

b. Gate drive resonant components

Fig 28. PFC and half-bridge MOSFET driver diagram

The capability of the IC MOSFET drivers are specified at the most interesting area (where the external MOSFETs are in the linear region).

I_{SOURCE} = −90 mA at V_{GS} = 4 V

R_{SINK} = 16 Ω at V_{GS} = 2 V

The sink resistance of 16 Ω is useful to damp the oscillation that can occur at the NMOST gate when the NMOST is switched off. In Figure 28b, L_S is the total inductance (track and source), C_{ISS} is the input capacitance of the NMOST as specified in the NMOST data sheet and R_G is the total series resistance (of the driver and of the NMOST).

Damping factor ξ of this series $R_G L_S C_{ISS}$ circuit is shown in Equation 31.

$$\zeta = R_G \times \frac{SQRT \times \left(\frac{C_{ISS}}{L_S}\right)}{2} \quad (31)$$

For sufficient damping, ξ must be greater than 0.5 (ideally >1).

A total inductance of 85 nH (21 nH ideally) can be supported without oscillation for a typical value for C_{ISS} = 330 pF and a value of 16 Ω for R_{SINK}.

3.15.1 VDD supply load

The major part of the power consumption from supply VDD is the gate drive. The amount of energy needed is linear to the switching frequency; the relationship is shown by Equation 32.

$$\Delta I_{VDD(PFC)} = Q_{g(PFC)} \times f_{PFC} \quad (32)$$

Where $Q_{g(PFC)}$ is the total gate charge as specified in the NMOST data sheet which is needed to charge the gate to the VDD supply voltage.

Note that there is also gate charge needed for the two half-bridge NMOSTs which are not synchronized to PFC switching.

The GPFC track contains large current spikes; ensure that next to the GPFC track a low-ohmic return ground is present in the layout. The track width determines the inductance per cm, therefore use wide tracks for gate drive signals in case large NMOSTs are used. The ground track next to the signal track also reduces the inductance per cm.

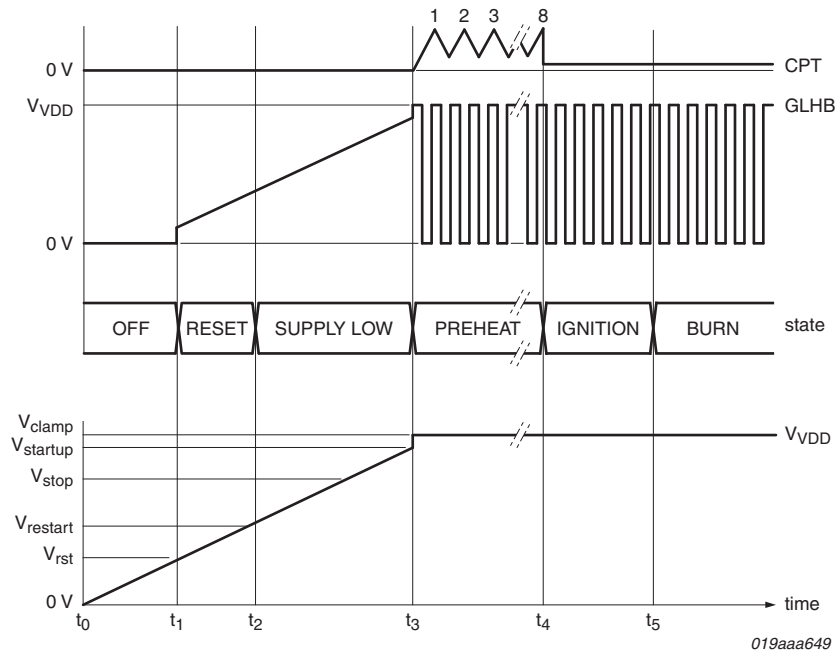
3.16 Pin GND: IC ground reference

This is the reference ground for the IC. Try to isolate the small signal ground and the large signal (gate drive currents, half-bridge switching currents and PFC switching currents) in the PCB layout.

3.17 Pin VDD: IC supply and gate drive supply

The application diagram for pin VDD is shown in Figure 30.

Refer to Figure 29. At power-on, the VDD supply determines when the IC starts oscillating. Initially the VDD capacitor is charged by the startup current. The VDD voltage rises and passes the threshold V_{rst} = 4.2 V; the gate drive signal of the low side switch is initially equal to VDD in order to charge the floating supply capacitor C24 via the internal bootstrap diode.



(1) Time t0: start charging VDD capacitor.

(2) Time t3: start oscillation, VDD takeover supply active.

(3) Time t4: preheat timer end.

(4) Time t5: lamp-on detected, transition to burn state.

Fig 29. Normal startup behavior

At the moment V_{VDD} passes the threshold $V_{startup}$ = 12.4 V, the gate drivers become active and Preheat state is entered. In Preheat state, capacitor C20 in the VDD takeover supply must deliver the energy to the IC and gate drivers.

Capacitor C20 is part of the dVdt supply that connects to the half-bridge switching node SHHB. On each rising edge of the SHHB node a current is fed through C20 and diode D13b to the buffer capacitor C23. The amount of current is determined by the value of capacitor C20.

If C20 has a high value (> 470 pF) it is advised to replace D13a by a 14 V Zener diode (1N5244) in order to remain within the V_{DD} voltage limits.

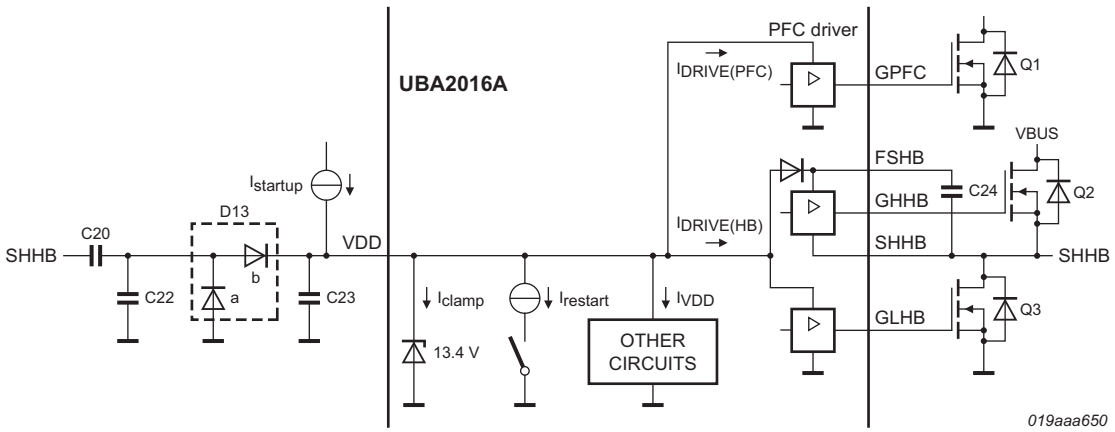


Fig 30. Pin VDD application

The VDD current consumption depends on the state of the IC.

- Stop (standby), Reset and Supply LOW state: The current consumption is 250 μA_{typ}.
- Preheat, Ignition and Burn state: Both PFC and HBC are switching. The MOSFET drivers are dominant in current consumption. Initially the VDD current is delivered by the energy in VDD buffer capacitor C23 but the dVdt supply circuit takes over. The current consumption (excluding the MOSFET driver) is 1.7 mA_{typ}. For typical FETs in a 35 W application the VDD current is 10 mA.
- Auto-restart state: The current consumption is 800 μA_{typ}. This current overrules the current $I_{startup}$ and the VDD capacitor is discharged. This state is used for multiple ignition attempts.

3.17.1 dVdt capacitor

The VDD supply current is mostly determined by the NMOST types and internal drivers, a small part (only 1.7 mA) is needed for internal circuitry.

Capacitor C20 is calculated by Equation 33.

$$C20 = 1.3 \times \frac{(2 \times Q_{g(HB)} + Q_{g(PFC)} + I_{VDD})}{VBUS} \quad (33)$$

Where factor 1.3 is a margin, $Q_{g(HB)}$ and $Q_{g(PFC)}$ are the total gate charges of the HB and PFC NMOST; VBUS is the bus voltage, I_{VDD} = 1.7 mA and $f_{low(HB)}$ = 40 kHz or 20 kHz in case of boost.

Note that the calculated value is the minimum value for capacitor C20, a typical value is 330 pF. The margin in the formula depends on the tolerances in the design. Take care not to exceed maximum current $I_{clamp(VDD)}$ = 20 mA of the internal clamp. Therefore never add too much capacitance to the calculated minimum value C20, or place a Zener diode of 13 V at position D13b in order to reduce the clamp current in the internal clamp.

3.17.1.1 Buffer capacitor

A buffer capacitor C23 is required at pin VDD. Current peaks can be localized by placing an SMD ceramic capacitor at position C23, close to the IC. The value of C23 should be approximately 100 times larger than the total gate capacitance of all MOSFETs to prevent significant voltage drop during the discharge time of C23. The value of C23 is calculated by Equation 34.

$$C23 > \pm 100 \times (2 \times Q_{g(HB)} + Q_{g(PFC)}) \quad (34)$$

A typical capacitor for C23 is a 470 nF, 0805, 50 V, X7R ceramic type.

3.17.1.2 Startup bleeder resistor

This resistor connects to the PFC output bus voltage or the Double-Sided Rectified (DSR) mains. The bus capacitor holds the bus voltage and is only slowly discharged by the bleeder resistor, so DSR mains connection is preferred. The DSR mains connection results in a shorter off-time in a power-on-off-on cycle.

The startup current must be sufficient to supply the $I_{standby(VDD)}$ = 240 μA. The startup current must be lower then $I_{restart(VDD)}$ = 800 μA otherwise the IC cannot leave the Auto-restart state. The startup current is calculated by Equation 35.

$$I_{startup} = 1.2 \times I_{standby(VDD)} \quad (35)$$

The ballast mains start voltage $V_{ac(start)}$ must be below $V_{ac(min)}$ RMS as shown in Equation 36.

$$V_{ac(start)} = 0.9 \times V_{ac(min)} \quad (36)$$

The startup bleeder resistor R31 that determines the startup current ($I_{startup}$) is calculated by Equation 37.

$$R31 = \frac{SQRT(2) \times V_{ac(start)}}{I_{startup}} \quad (37)$$

The GLHB is 12 V in standby state in order to pre-charge the floating supply capacitor on pin FSHB. This could interfere with the detection of the hot side lamp electrode if the circuit is not properly designed.

3.18 Pin GLHB: Low-side half-bridge gate driver

The application for this pin is identical to pin GPFC; see Section 3.15 on page 35.

The GLHB is 12 V in standby state in order to pre-charge the floating supply capacitor on pin FSHB. This must be noted when designing a ballast that must detect the hot side filament of the lamp.

It is recommended to connect the gate of the lower half-bridge MOSFET to pin GLHB via a small series resistor to prevent oscillation caused by parasitics. This oscillation will increase stress on the MOSFETs. Do not use a too high resistor value to prevent switching the MOSFET on via it's Miller capacitance.

3.19 Pin SHHB: hard switching, capacitive mode, ground of high-side driver, source of the dVdt supply

In normal operation, the half-bridge is Zero-Voltage-Switching (ZVS), which means that the SHHB circuit node has commuted before the NMOST switches on. The SHHB node capacitance is charged or discharged by the current of the half-bridge inductance; the impedance of the half-bridge circuit is “inductive”. However, at low operating frequencies (overpower) or sudden removal/damage of the load (lamp) the impedance of the half-bridge circuit can become “capacitive”; there will be no commutation current because the impedance is capacitive.

3.19.1 Hard switching

ZVS is assumed if the voltage step on the SHHB node is below 30 V.
If the voltage step on the SHHB node is above 100 V then hard switching is assumed.

3.19.2 Capacitive mode

Capacitive mode protection is triggered when the voltage rise during the non-overlap time of the low-to-high transition of the SHHB node remains under $V_{th(cm)(SHHB)}$ = 30 V/μs.

If the slope of the voltage rise is > 30 V/μs, then hard switching or ZVS can be assumed.

3.20 Pin FSHB: supply for high-side driver

Pin FSHB must be connected to pin SHHB via capacitor C24. The capacitor must hold the charge for the internal high-side driver. The supply structure is shown in Figure 30 on page 38.

When SHHB is switched to GND by the external low-side power switch (GLHB is HIGH) current flows via the bootstrap internal diode and high-voltage switch into C24. The high-side driver is supplied from this capacitor when SHHB is above GND. The voltage drop across the internal diode and high-voltage switch is $V_{fd(bs)}$.

A typical value for C24 is 100 nF which is sufficient for most applications.

3.21 Pin GHHB: High-side half-bridge gate driver

The application for this pin is identical to pin GPFC; see Section 3.15 on page 35.

It is recommended to connect the gate of the higher half-bridge MOSFET to pin GHHB via a small series resistor to prevent oscillation caused by parasitics.

4. Application description

4.1 Power supply

The power supply to the IC includes several functions:

- Clamping by the internal clamping diode
- Restart internal current source
- Supply of the IC drivers function
- Supply of the IC controller function blocks

4.1.1 IC supply structure overview

Pin VDD is the power supply pin. Internally the supply pin is clamped to 13.4 V by the integrated clamp and excessive VDD current (I_{clamp}) is removed. The 13.4 V is used for the internal circuitry and for the integrated MOSFET drivers. An integrated bootstrap diode supplies the GHHB driver.

Pin VDD must be connected to an external buffer capacitor which can be charged from one of several sources:

- Charge current $I_{startup}$ from the bus voltage
- A dVdt supply connected to the half-bridge
- Auxiliary supply from a winding on the half-bridge transformer
- External DC supply from a standby supply

4.1.2 Startup

It is possible to restart after a re-lamp action without a ballast power cycle of the ballast if the startup current is fed through the lamp filament at Restart.

4.1.3 Restart

To provide multiple ignition attempts, the Auto-restart state is implemented. During the Auto-restart state the IC is not oscillating and there is an extra current ($I_{restart}$ = 800 μA) drawn from VDD. When $I_{restart}$ is larger then $I_{startup}$ a restart is triggered when the VDD drops below $V_{restart(VDD)}$ = 6.2 V. The restart timing depends on C23 and $I_{startup}$.

4.1.4 Stop

The IC stops operating when the VDD voltage drops below $V_{stop(VDD)}$ to prevent unreliable switching of the half-bridge and PFC circuit. The IC enters Supply-low state.

4.2 Choice of the VBUS voltage

In order for the PFC step-up converter to work correctly, the bus voltage must be higher than the maximum input voltage, calculated by Equation 38.

$$VBUS > 1.1 \times \sqrt{2} \times V_{ac(max)} \quad (38)$$

At the lowest HB switching frequency the bus voltage must be sufficient to reach the required lamp current with an HB inductance, calculated by Equation 39.

$$VBUS > \sqrt{3} \times 8 \times f_{hb(min)} \times L_{hb(res)} \times I_{lamp(max)} \quad (39)$$

At the nominal HB switching frequency, the bus voltage must be sufficiently high to support the required lamp voltage as shown by Equation 40.

$$VBUS > \frac{V_{lamp(nom)} \times pi}{\sqrt{2}} \quad (40)$$

The three formulas above provide a minimum value for VBUS, it is advised to choose that value.

4.3 PFC stage design

The maximum switching frequency $f_{high(PFC)}$ is limited by the $t_{off(low)}$ parameter; the minimum switching frequency $f_{low(PFC)}$ is a design parameter. It is advised to keep $f_{low(PFC)}$ above the audible range for humans and animals (30 kHz) during normal operation.

Normal operating voltage range: $V_{ac(rms)(min)}$ to $V_{ac(rms)(max)}$.

Nominal power: PF > 0.9 and $f_{low(PFC)}$ > 30 kHz.

The inductance L_{PFC} can be calculated for a certain $f_{low(PFC)}$ as shown in Equation 41.

$$L_{PFC} = \frac{V_{ac(rms)(max)}^{2} \times (VBUS - \sqrt{2} \times V_{ac(rms)(max)})}{2 \times f_{low(PFC)} \times \frac{P_{lamp}}{\eta} \times VBUS} \quad (41)$$

Remark: If the boost function is used over the complete input voltage range, the P_{lamp} must be the maximum lamp power during boost.

The calculation of the maximum peak current $I_{pk(max)(PFC)}$ of the PFC inductor operating in critical conduction mode is calculated by Equation 42.

$$I_{pk(max)(PFC)} = \frac{2 \times \sqrt{2} \times \frac{P_{lamp}}{\eta}}{V_{ac(rms)(min)}} \quad (42)$$

Application requirements: Efficiency η = 0.9; P_{lamp} = 49 W; $V_{ac(rms)(min)}$ = 180 V to give: $I_{pk(max)(PFC)} = 856\ mA$

Valley-detection needs additional ringing time within every switching-cycle. The ringing time adds short periods while no power is transferred to the PFC output. The PFC controller compensates for this with a slightly higher peak current. A rule of thumb is that the peak current in a boundary condition mode, PFC with valley skipping is a maximum of 10 % higher than the calculated peak current in boundary conduction mode as shown in Equation 43.

$$I_{LPFC(sat)} = 1.1 \times I_{pk(max)(PFC)} \quad (43)$$

The RMS current in the PFC inductor is calculated by Equation 44.

$$I_{LPFC(rms)} = 2 \times \frac{P_{lamp}}{SQRT(3) \times V_{ac(min)} \times \eta} \quad (44)$$

Once the inductance L_{PFC} and saturation current $I_{pk(max)(PFC)}$ are known, the PFC inductor can be designed. The design requirements must include the following:

- Inductance
- Saturation current at maximum operating temperature
- Maximum RMS current to determine the temperature increase
- Switching node close to core for low EMI
- Winding ratio primary: auxiliary

The winding ratio calculation is described in Section 3.14 on page 34 and shown as: $(Np)/(Ns) = 0.11 \times VBUS$.

The low frequency output voltage peak-to-peak ripple is calculated by Equation 45.

$$VBUS_{(pk-pk)} = \frac{P_{lamp}}{2 \times \pi \times f_{ac} \times VBUS \times C_{BUS}} \quad (45)$$

Where $VBUS_{(pk-pk)}$ is usually chosen to be from 10 % to 15 % of VBUS.

Once the ripple currents are measured in the application for certain capacitor values, the capacitor manufacturer can help support life-time calculations.

Suggested capacitor series for ballast applications are: Rubicon BX series, Nippon KXG and Panasonic EB type A.

4.4 Half-bridge

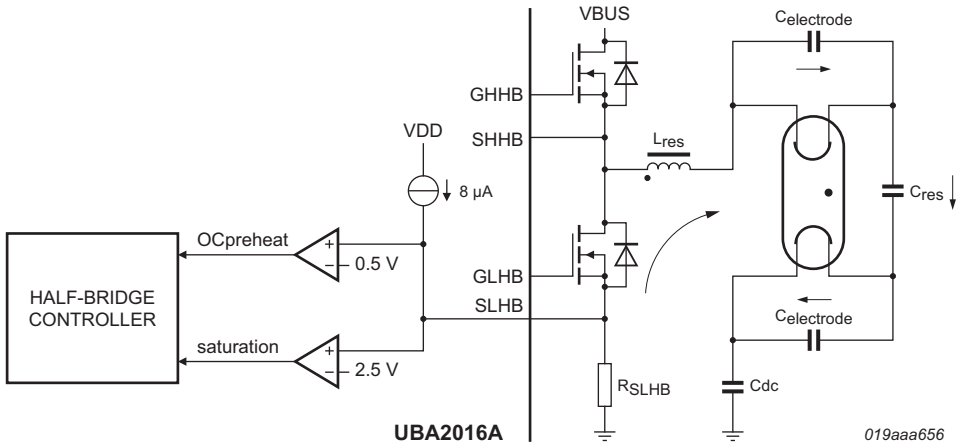
The basic half-bridge circuit consists of an LC tank. Before the lamp is ignited, the LC tank is not damped and the voltage across the lamp strongly depends on the switching frequency. Electrode heating is applied while the lamp voltage is below the ignition voltage and the switching frequency is above the resonant frequency. After preheating, the lamp is ignited by sweeping the switching frequency down towards the resonant frequency. After ignition (Burn state) the lamp acts as a resistive load on the LC tank. The inductor limits the current though the lamp.

There are several topologies for heating the lamp electrodes. The conventional and inductive heating is addressed in the following sections.

4.4.1 Conventional heating

See Figure 31. In Preheat state, the half-bridge current flows through Cdc, C_{res} and the electrodes of the lamp (except a small amount which flows through C electrode). Once the lamp is ignited, the half-bridge current also flows through the lamp and the resonant tank (Lres Cres) is damped.

This type of circuit is used when lamp current control is not required. The switching frequency is set by the half-bridge controller.



L_{res}: limits the lamp current in normal operation.

C_{res}: generates the ignition voltage.

$C_{electrode}$: reduces the electrode current in nominal operation.

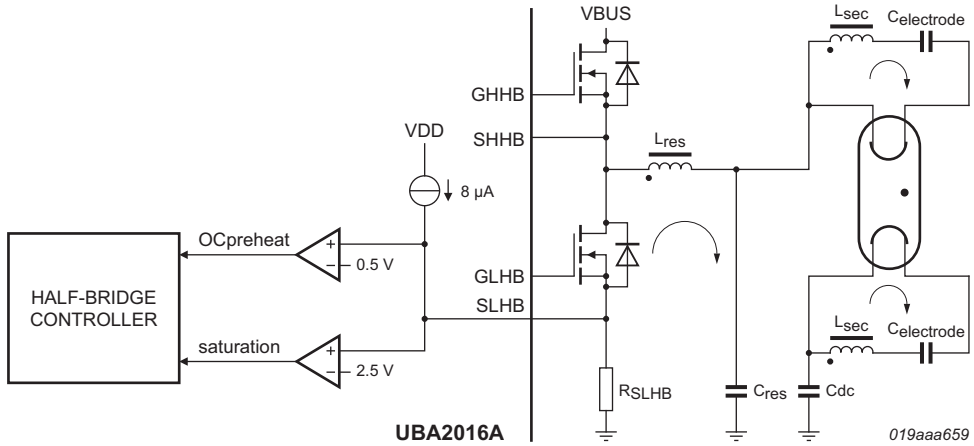
R_{SLHB}: limits the half-bridge current during preheat and sets the saturation current.

Fig 31. Pin SLHB and conventional heating

4.4.2 Inductive mode heating

See Figure 32. In Preheat state, the half-bridge current flows through L_{res} and the electrodes of the lamp (no current flows through Cdc). Once the lamp is ignited, the half-bridge current also flows through the lamp and the resonant tank ($L_{res}C_{res}$) is damped. The current though the Cdc capacitor is equal to the lamp current, as a result the lamp current can easily be measured.

This type of circuit is used if lamp current control is required, such as dimming.



L_{res}: inductor coupled to L_{sec}, limits the lamp current in normal operation.

C_{res}: generates the ignition voltage.

$C_{electrode}$: reduces the electrode current in nominal operation.

L_{sec}: inductor coupled to L_{res}, determines the amount of electrode current.

R_{SLHB}: limits the half-bridge current during preheat and sets the saturation current.

Fig 32. Pin SLHB and inductive heating

4.4.3 Half-bridge current control

Saturation regulation level is a fixed ratio (5×) to the preheat regulation level. The saturation level must support worst case (cold and old lamp) ignition voltages.

If the default application (factor 5) is selected, the preheat current through the half-bridge is: $I_{worstcase(ignition)} < 5 \times I_{ph}$; see Figure 33.

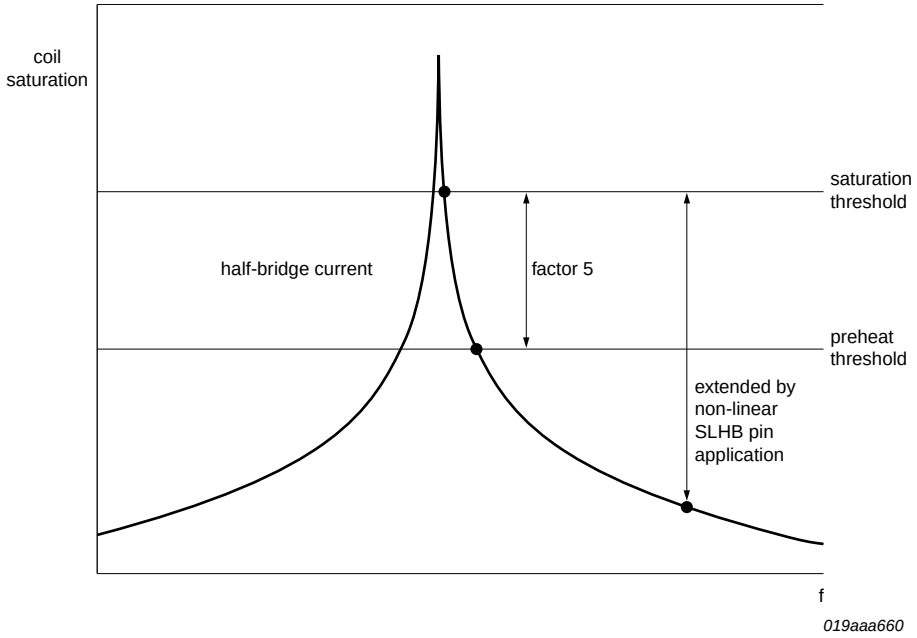


Fig 33. Relationship between coil saturation and preheat current

4.5 Layout guide

Figure 34 is an application example of a dual-layer PCB where the component-side layer tracks are Grey and the soldering-side tracks are Red, Blue and Cyan. The Blue track is the ground plane, a part of which is used as a small signal ground. This small signal ground is highlighted in Cyan. This ground is used for the components listed below in order to minimize the pickup of noise in case of deep dimming and ignition. Therefore, for this reason it is recommended to route the IFB track next to a ground plane or track.

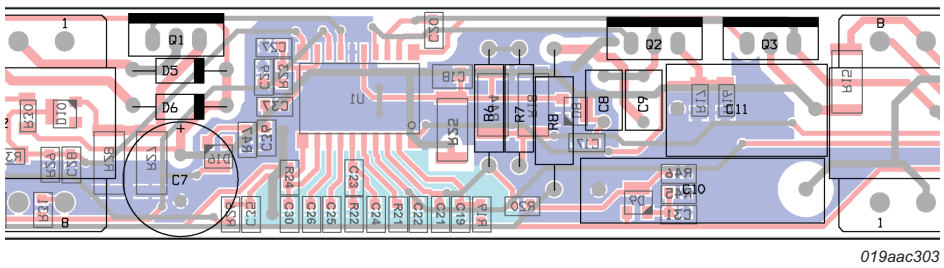


Fig 34. Top view of dual-layer PCB for an application example using UBA2016A in an SO20 package

A separate small signal ground is recommended for the following:

- Pin 2, IFB: C19
- Pin 3, EOL: C21
- Pin 4, VFB: C22
- Pin 5, IREF: R21

- Pin 6, CIFB: R22, C24
- Pin 7, CF: C25
- Pin 8, CPT: C26
- Pin 9, DIM: C30
- Pin 10, BOOST, C30

Figure 35 is an example of an application of a single-layer PCB whose tracks are shown Red, Blue and Cyan. The Blue track is the ground plane, a part of which is used as a small signal ground. The small signal ground is highlighted in Cyan and is used for the following components in order to minimize the pickup of noise in case of ignition. IFB is connected to ground because this is a non-dimmable application.

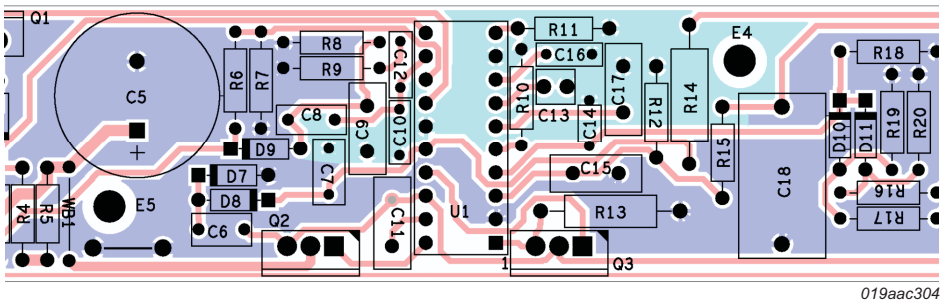


Fig 35. Top view of a single-layer PCB for an application example using UBA2015 in a DIP20 package

A separate small signal ground is recommended for:

- Pin 3, EOL: C15
- Pin 4, VFB: C14
- Pin 5, IREF: R10
- Pin 6, CIFB: C17
- Pin 7, CF: C13
- Pin 8, CPT: C16
- Pin 10, PH/EN, R11
- Pin 15, GND
- Pin 16, VDD: C7

4.6 Tips and tricks

4.6.1 PFC disable

The PFC controller can be disabled using the options shown in Table 7.

Table 7. PFC disable options

Shows the options for disabling the PFC controller for experimental purposes.

Pin connection			PFC mode	PFC behavior
AUXPFC	COMPPFC	FBPFC		
GND	n.a.	n.a.	no demagnetization detected	GPFC pulses with minimum pulse width
Open	n.a.	n.a.	freeze	GPFC remains LOW, minimal current consumption and no disturbance
n.a.	FBPFC	COMPPFC	n.a.	FBPFC regulates to approximate 1.1 V, disabled protection: brownout, FBPFC, OSP, FBPFC, overvoltage, EOL window changes
n.a.	GND	1.27 V	n.a.	FBPFC must be set externally to 1.27 V from bus voltage for normal EOL window, disabled protection: brownout, FBPFC, OSP, FBPFC, overvoltage, EOL window changes

4.7 Power-on of new ballast design

4.7.1 Test 1: check for short-circuits

Apply voltage to pin VDD via 330 Ω resistor and 20 V lab supply.

Start-up the supply from 0 V and monitor the current and voltage on pin VDD.

The voltage should clamp at about 13 V to 14 V. Do not increase VDD above 14 V or permanent damage may occur.

4.7.2 Test 2: check if oscillation stage is reached

Switch VDD supply to 0 V.

Apply 1.27 V to pin FBPFC to enable switching of the MOSFETs.

Increase VDD until its clamped, when using 330 Ω in series, the lamp supply can be increased to less than 20 V while keeping the internal clamp within specification.

The gate drive signals (PFC and half-bridge) should show some activity when the VDD passes the startup threshold.

4.7.3 Test 3: check half-bridge functionality

Switch VDD and FBPFC to 0 V.

Connect diode to pin CPT and connect its cathode to ground, to disable the preheat and fault timer.

Apply 1.27 V to pin FBPFC and 12.9 V to pin VDD.

Connect a 400 V lab supply to the bus capacitor and set the current limit to 200 mA.

Slowly increase the bus voltage from 0 V to between 20 V and 30 V, and monitor the lab supply current. Monitor the bus voltage (PFC output voltage) and the source high-side of the half-bridge. Monitor the voltage across the resonant capacitor: the average voltage must be VBUS / 2.

4.7.4 Test 3: check half-bridge functionality

Remove VDD, FBPFC and bus lab supply.

Remove diode from pin CPT.

Connect 400 V, DC lab supply to the AC input, and set the current limit to 200 mA.

Slowly increase the lab supply voltage from 0 V to between 20 V and 30 V, and monitor the lab supply current and the VDD voltage.

Check if PFC starts regulating if the FBPFC voltage > 1.0 V.

4.7.5 VFB disable

Connect a lab supply of 500 mV to pin VFB. Make sure that the lamps are inserted because high voltage can occur in the LC tank.

4.7.6 EOL disable

Connect a lab supply of 1.9 V to pin EOL.

5. Abbreviations

Table 8. Abbreviations

Acronym	Description
EMI	ElectroMagnetic Interference
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NMOST	N-channel Metal Oxide Semiconductor Transistor
SMD	Surface-Mounted Device
VCO	Voltage-Controlled Oscillator

6. References

[1] UM10359: UBA2016AT HFTL demo board with boost and dimming.

[2] UM10439: UBA2015P reference design 230 VAC (two T5 lamp ballast non-dimmable).

7. Legal information

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